Part #0802-0076

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MODEL 802

TRANSIENT RECORDER

OPERATING AND SERVICE MANUAL

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OPERATING & SERVICE MANUAL
Model 802

Table of Contents

Section

I General Information
- 1.1 Certification and Warranty
- 1.2 Instrument Description
- 1.3 Specifications

II Installation
- 2.1 Introduction
- 2.2 Unpacking and Inspection
- 2.3 Storage and Shipment
- 2.4 Power Connections
- 2.5 Preparation for Use
- 2.6 Initial Warmup

III Principles of Operation
- 3.1 Introduction
- 3.2 Basic Circuit Description
- 3.3 Triggering
- 3.4 Modes of Operation
- 3.5 Circuit Limitations

IV Operation
- 4.1 Introduction
- 4.2 Front Panel Controls
- 4.3 Rear Panel Connectors
- 4.4 Setup Procedures
- 4.5 Operation Procedures
  - 4.51 Trigger Hold-off
  - 4.52 Delayed Sweep
  - 4.53 Switched Time Base
  - 4.54 Pretrigger Record

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Section

V Output Interface

5.1 Introduction

5.2 Analog Interface and System Calibration

5.21 Oscilloscope Interface

5.22 X-Y Display

5.23 Plotter Interface

5.3 System Calibration

5.4 Digital Interface

5.41 Data Format

5.42 Data Availability

5.43 Data Output Rates

5.44 Output Control Sequence

5.5 Remote Programming and Sensing

5.6 External Time Base

5.7 Rear Panel Signal Call-out

VI Calibration & Maintenance

6.1 Introduction

6.2 Required Test Equipment

6.3 Setup Procedure

6.4 Power Supplies

6.5 Input Amplifier

6.6 Analog/Digital Converter

6.61 First Rank ADC

6.62 Second Rank ADC

6.7 Linear Board

6.71 Digital-to-Analog Converter

6.72 Delay

6.73 X Ramp

6.8 Time Base Register Rates & Frequencies

6.9 Disassembly Procedure

6.91 Front Panel

6.92 Power Supply

6.10 Plot Output Rate Adjustment

Section

VII Theory of Operation & Circuit Description

7.1 Theory of Operation
7.2 Front Panel
7.3 Input Amplifier
7.4 Analog-to-Digital Converter
7.41 First Rank Converter
7.42 Second Rank Converter
7.5 Control #1
7.6 Control #2
7.7 Memory
7.8 Linear
7.9 Time Base & Address
7.10 Power Supply
7.11 Mother Board

CERTIFICATION

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

WARRANTY

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defected during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

1.2 Instrument Description

The Model 802 Transient Recorder is a compact, lightweight, solid state electronic instrument which stores the digital equivalent of electrical waveforms in a memory. The outputs of the Model 802 can be interfaced to display instruments such as oscilloscopes, CRT displays, plotters or strip chart recorders. It can also be interfaced directly to digital computers, disc and magnetic tape storage devices, etc., as a data acquisition device.

The Model 802 is a bench-type instrument with tilt-up stand and may also be rack mounted, occupying one-half rack width and 5-1/4 inches of vertical space.

Specifications for the Model 802 are shown on the following page.

TECHNICAL SPECIFICATIONS

INPUT CHARACTERISTICS

Input Impedance	1 megohm ‖ 50 pf.
Input Range	10 mV to 50 V full scale.
Input Resolution	0.4% or 1 part in 256 for full scale input.
Input Offset	±1.5 X full scale input range. Light indication when part of signal is offscale.
Maximum Input Level	±100 V.
Frequency Response	DC to 500 KHz all ranges (3 db point; AC coupling provides low frequency cutoff of 2 Hz).
Sweep Time, Sweep A or B	500 μsec to 20.0 sec for the first 1000 words.
Sweep Time, External	External advance of sweep. Pulse of +5 V to 0 V, risetime <100 nsec, advances memory one step. Rate continuously variable from 2 μsec to 500 μsec per address. If delay of more than 500 μsec occurs between advance pulses, all further pulses will have 2000 μsec latency.
Internal Calibration	Signal provided to record independent of the sweep time selected. Useful for setup of scope display or YT recorder.

TRIGGERING CHARACTERISTICS

Modes of Operation	
Auto	Sweep is initiated every 100 msec in the absence of a trigger (useful primarily during setup).
Normal	Sweep initiated by each acceptable trigger.
Single	Sweep initiated by each acceptable trigger only after arming by pushbutton switch or by remote arm input.
Trigger Selection	
Source: Internal	Trigger obtained from input signal.
External	External trigger required.
External ÷ 10	External trigger input attenuated by 10.
Slope	Positive or negative selectable.
Level	0 to ±5 V adjustable.
Trigger, Internal or External	
Pulse Width	>100 nsec.
Pulse Height	>400 mV.
Trigger Coupling	
DC	DC coupling.
AC Slo	20 Hz to 30 kHz.
AC	15 kHz and above.
Trigger Delay	0 to 10X sweep time (nominally) to a maximum of 10 sec, continuously variable.
Modes of Operation	
Trigger Holdoff	Next trigger (Normal mode) not acceptable until after delay period set with 10 turn control.
Delayed Sweep	Sweep start is delayed from trigger by the delay period set with 10 turn control.
Pretrigger Recording	Recording is continuous until trigger is received, at which time delay period starts. End of delay period stops recording process so that signal received prior to end of trigger plus delay period is held in memory.
Switched Time Base	Sweep Time A is used for initial portion of sweep. Switch to Sweep Time B after delay selected on 10 turn delay control. Sweep Times A and B are set independently. Change-over point continuously variable
Delay Stability (short term)	±1% of sweep time or 1% of delay, whichever is greater.

FUNCTIONAL CHARACTERISTICS

A/D Converter	8 bit, 50 Hz to 2 MHz word conversion rate, depending upon sweep time selected.
Time Base	10 MHz crystal controlled oscillator

OUTPUT INTERFACE

Output Signal	
Analog X Axis	1 V full scale ±1.5 V offset.
Display Expand	X1, X5, X10.
Analog Y Axis	1 V full scale ±1.5 V offset
Digital Information	8 bit parallel TTL level, positive true.
Digital Address	10 bit parallel TTL level, positive true
Switched Time Base Point	1 bit TTL level, positive true.
Input Range, Sense	6 line parallel, 0 to +2 V, positive true, 1 K source impedance, 10 K minimum load.
Input Range, Control	6 line parallel, 0 to +4 V, maximum source impedance 500 Ω.
Sweep Time A, Sense	7 line parallel, 0 to +2 V, positive true, 1 k source impedance, 10 K minimum load.
Sweep Time A, Control	7 line parallel, 0 to +4 V, maximum source impedance 500 Ω.
Sweep Time B	Not available digitally.
Output Sweep Speed	
Analog Y Axis	2 msec for oscilloscopes, 100 sec for YT recorder.
Analog X Axis	2 msec only.
Digital	2 μsec to 500 μsec/address, 2 msec latency for asynchronous rates slower than 500 μsec/point. Digital output starts at fast rate. If delay of more than 500 μsec occurs between command pulses, all further points will have 2 msec latency.

DIGITAL INTERFACE SIGNALS

Output Command	TTL, +5 V to 0 V and held at 0 V to provide digital output operation.
Flag Output	
Level	TTL, 0 to +4 V, risetime <100 nsec.
Pos. Transition	New data available in output buffer
Neg. Transition	Command has been received and should be removed.
Word Command	
Level	TTL, +5 V to 0 V, risetime <100 nsec.
Neg. Transition	Requests next word to be placed in buffer.

MISCELLANEOUS

Operating Temp. Range	0-55°C
Power	100-130 or 200-260 V AC, 50 W, 50-60 cycles.
Size	Height 5.25 inches, width 8.5 inches, depth 17 inches.
Weight	18 lbs., shipping weight 25 lbs.

SECTION II

Installation

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage and installation of the Model 802.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. A performance check for the instrument is given in Section IV on Operation. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Palo Alto, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

Line voltage: the Model 802 may be operated from either 115 or 230 volt (±10%) power lines. A slide switch on the rear panel permits quick conversion for operation from either voltage. Insert a narrow-blade screwdriver in the switch slot and slide the switch to the left for 230 volt operation ("230" marking exposed), or to the right for 115 volt operation ("115" marking exposed). The Model 802 is supplied with a 115 volt fuse, 1 amp, slow blow; be sure to replace this fuse for 230 volt operation with a 0.5 amp slow blow fuse.

CAUTION: Before plugging instrument into AC power line, be sure slide switch is properly positioned.

Power cable: the Model 802 is equipped with a detachable 3-wire power cable. Proceed as follows for installation.

A. Connect flat plug (3-socket connector) to AC line jack at rear of instrument.

B. Connect plug (2-blade with round grounding pin) to 3-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 802 is not a "self-contained" instrument in that it must be interfaced with other types of instrumentation in order for the data to be visible or analyzed. The following sections of this manual cover operation, setups, and interface requirements.

2.6 Initial Warmup

Although the Model 802 is a solid state instrument, a brief warmup period of approximately 10 minutes is required for the input amplifier and the analog-to-digital converter to reach thermal stabilization. This warmup period is recommended for both the Model 802 and its associated output device.

SECTION III

Principles of Operation

3.1 Introduction

The Transient Recorder is a new class of electronic instrument using digital techniques to record a preselected section of an analog signal as it varies with time. Thus, the waveshape during the selected period of time is recorded and held in the instrument's memory until a new recording is made or power is removed. While the information is stored in the instrument's memory, it can be (1) viewed as a reconstructed analog signal on an oscilloscope or X-Y display, (2) output as a reconstructed analog signal to a strip chart or YT recorder for making a permanent paper record, or (3) output in digital form to a digital recorder or directly to a computer for signal analysis or processing.

3.2 Basic Circuit Description

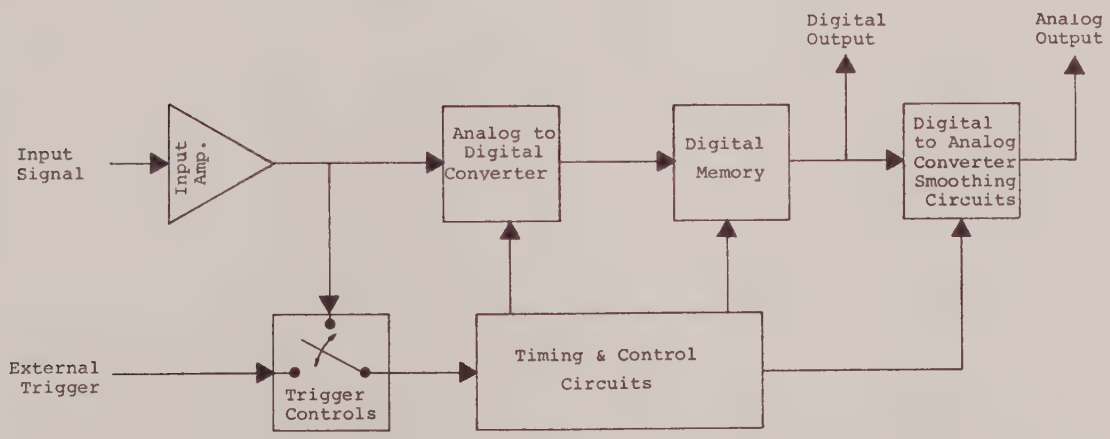


Figure 3.1

The Model 802 Transient Recorder operates as shown in Figure 3.1. A trigger to initiate the sweep can be provided externally or can be derived from the input signal itself using Trigger Level and Slope controls on the front panel. These controls are similar to those on most oscilloscopes.

The input signal is first amplified and then converted to its digital equivalent. The digital information is then stored in a semiconductor memory. Since only a fixed number of points (1024) can be stored in the memory, the front panel Sweep Time control determines the rate at which points are taken and equally spaces these points over the selected sweep time. The stored digital data can be output directly, or can be processed through a digital-to-analog converter and smoothing circuit to reconstruct the analog input signal for presentation on an oscilloscope, strip chart or YT recorder. Data in storage will remain there indefinitely until the instrument is instructed to make a new recording, in which case the new data replaces the old. Removing power from the instrument will erase the data from the memory.

3.3 Triggering Modes

Triggering of the Model 802 Transient Recorder is accomplished in a manner identical to that of most modern oscilloscopes. The two basic types of triggering action occur on Internal Trigger or External Trigger. The second degree of freedom is in whether or not the trigger is obtained from the positive or negative slope of the signal and, finally, the trigger level determines the point on the waveshape at which the trigger or recording sweep is begun.

In addition, there are three types of triggering modes: Single, Normal, and Auto. In the Single mode the trigger circuit must be armed by pressing the Arm pushbutton or by applying a pulse to the digital arm pin on the rear panel connector. When the trigger circuit is ready to accept a trigger signal, the arm lamp will be illuminated. Once a trigger has been received, the arm lamp will extinguish, indicating that the instrument has recorded new data or, in the case of the pretrigger record mode, that recording has stopped. Therefore, in the Single mode the trigger circuit must be manually armed each time before new data will be stored in the memory.

In the Normal trigger mode the trigger circuit will automatically be rearmed after each record and display cycle. Again in this mode the arm lamp indicates when a trigger has occurred.

In the Auto trigger mode the trigger circuit is triggered at a fixed rate of every 0.1 second. If a trigger signal is also available at the input and its rate is faster than 0.1 sec, it will override the automatic trigger. However, this mode is primarily useful during setup only.

Figures 3.2 and 3.3 show a typical input signal with the trigger levels indicated. Also shown in these figures are those portions of the input signal which would be stored in the memory of the Model 802.

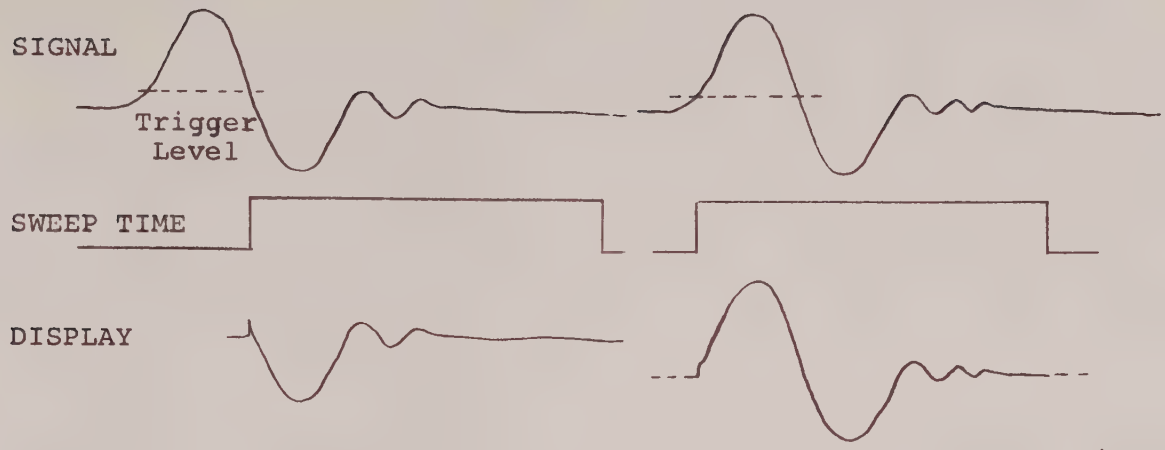


Figure 3.2a Internal Trigger - Slope

Figure 3.2b Internal Trigger + Slope

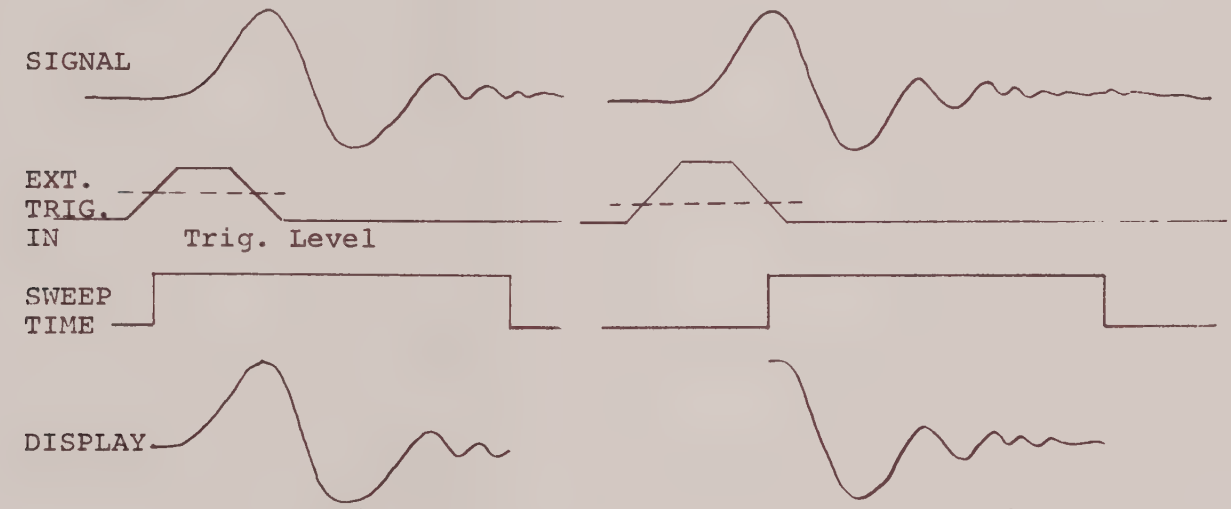


Figure 3.3a External Trigger + Slope

Figure 3.3b External Trigger - Slope

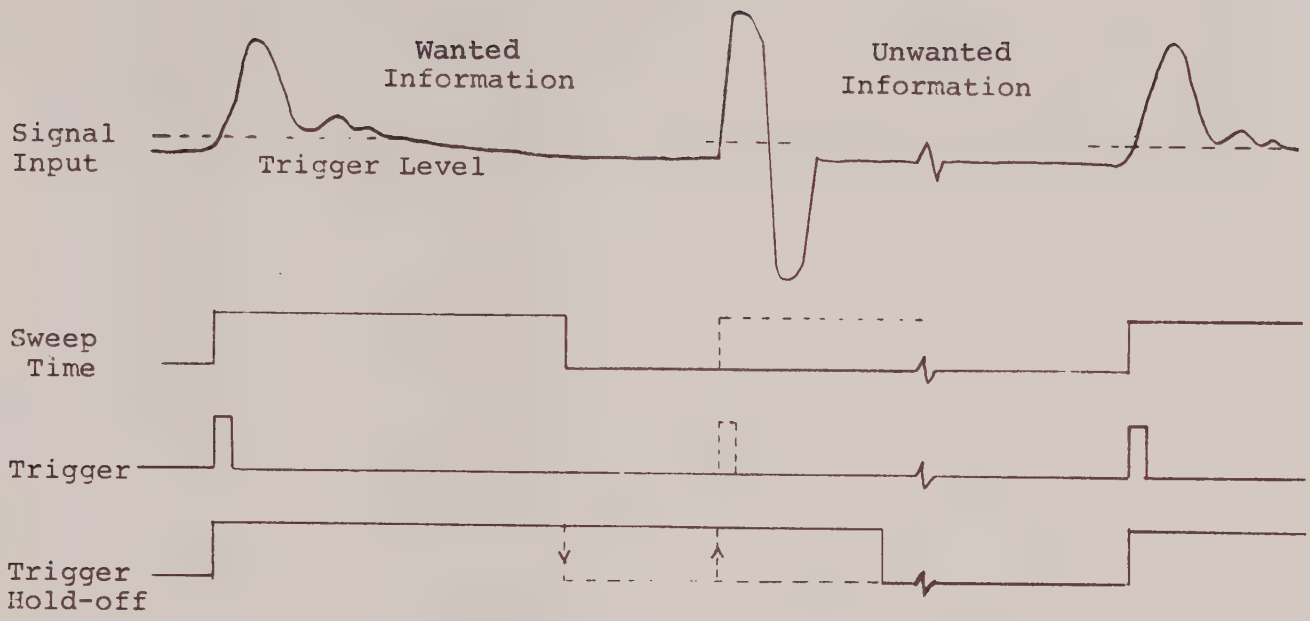
3.4 Modes of Operation

The Model 802 has four fundamentally different modes of storing data. The modes involve four different types of triggering situations. The selection of triggering modes is accomplished by the position of the front panel slide switch just to the right of the Delay control.

The four modes are referred to as: Trigger Holdoff, Delayed Sweep, Pretrigger Recording and Switched Time Base. These modes are described individually in the discussion below.

A. Trigger Holdoff.

This mode of operation is selected by moving the switch pointer to the "Trig Holdoff" position. Trigger Holdoff, simply stated, is a mode whereby dead time is added to the trigger circuit beyond the record time. Figure 3.4 illustrates a case where this would normally be used.



Dashed lines show undesirable event that would occur without the use of the Trigger Holdoff.

Figure 3.4 Trigger Holdoff

Suppose that one wants to examine a transient signal which occurs at low repetition rates. The objective is to see how this signal changes over a period of time. The triggering mode selected on the front panel would be "Normal". In this way each signal would be stored and displayed until the next signal came along to replace it. If the signal is a clean signal such that the only perturbations on the input line are those which are the object of the investigation, then there is no problem. However, it often occurs that following the legitimate signal there will be an unwanted perturbation which is capable of triggering the Model 802. In this case, the legitimate signal would be stored but when the perturbation came along the unit would be retriggered and the useful information immediately erased from memory.

As shown in Figure 3.4, the Delay control can be used to "hold off" the trigger beyond the unwanted perturbation so that the Model 802 will not retrigger until the end of the delay period. In this way the desired information will not be disturbed and the hold-off mode of operation will have been accomplished. Delay time of the trigger hold-off can be adjusted to approximately 10 times the sweep time, or 10 seconds, whichever is smaller.

B. Delayed Sweep.

The Delayed Sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the trigger and the desired information is greater than one sweep time. Therefore, the transient would not be captured with sufficient resolution to be useful. By delaying the sweep and operating at a faster sweep time, the information can be captured with good resolution.

Figure 3.5 illustrates a typical case where the unit is to be triggered externally but the information to be captured is delayed from the trigger. The Delay control in this mode of operation adjusts an internal delay such that the recording sweep does not start until the end of the delay period. The delay is adjustable from 200 nsec to approximately 10 times the sweep time, or 10 seconds maximum, whichever is shorter.

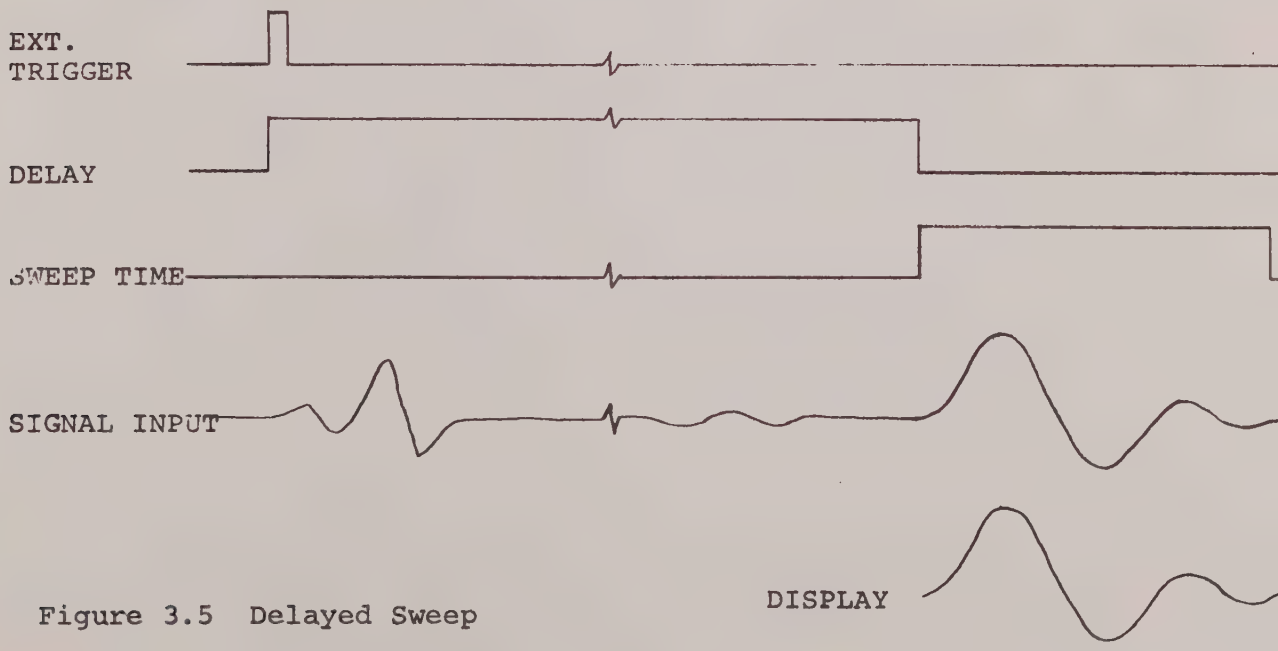


Figure 3.5 Delayed Sweep

C. Pretrigger Recording

Pretrigger Recording is a unique feature of the Model 802. It offers flexibility heretofore unavailable in any low cost instrumentation. Pretrigger Recording allows you to capture and record signals that you do not know you want to capture until the signal itself has passed. Another good use of this mode is in a case where the only good trigger available follows the information of interest.

In both of the two previous modes of operation the memory is filled with new information when the trigger signal occurs. In the Pretrigger Recording mode of operation the memory is constantly being filled with information but this information is being discarded at the same rate. When a trigger occurs, no more information is inserted into the memory and, likewise, no information is discarded. The memory then contains a block of information whose duration is equal to the sweep time. Since the memory is constantly storing and discarding information and stops storing upon receipt of a trigger, the information in memory would only be of value when the Single Sweep Trigger mode of operation is used.

With the Delay control set to its most counterclockwise position, the information stored in memory (upon receipt of the trigger) will represent an event occurring one sweep time preceding the trigger. In delaying the trigger, by means of the Delay control, it is then possible to record events occurring before, during and after the trigger signal. Use of this mode is illustrated in Figure 3.6. The Pretrigger Recording mode of operation offers many possibilities for doing biomedical work, electronic trouble-shooting, fault analysis of electrical or mechanical equipment, destructive testing monitoring, etc. This mode greatly enhances the overall usefulness of the Model 802 Transient Recorder. The delay is adjustable from 200 nsec to 10 times sweep time, or 10 seconds maximum, whichever is shorter. A delay less than one sweep time is normally used. If more delay is used, operation will be similar to the delayed sweep mode.

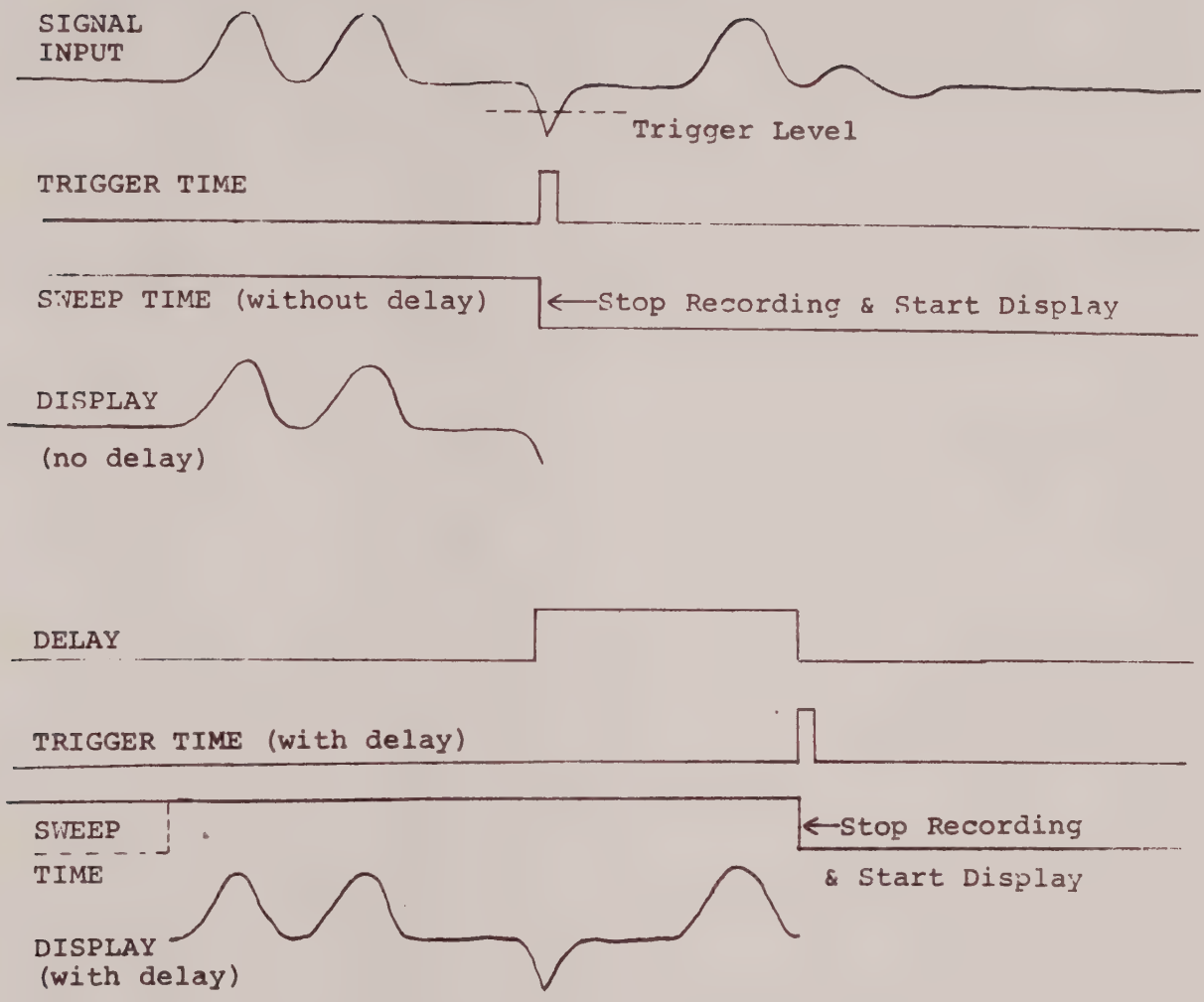
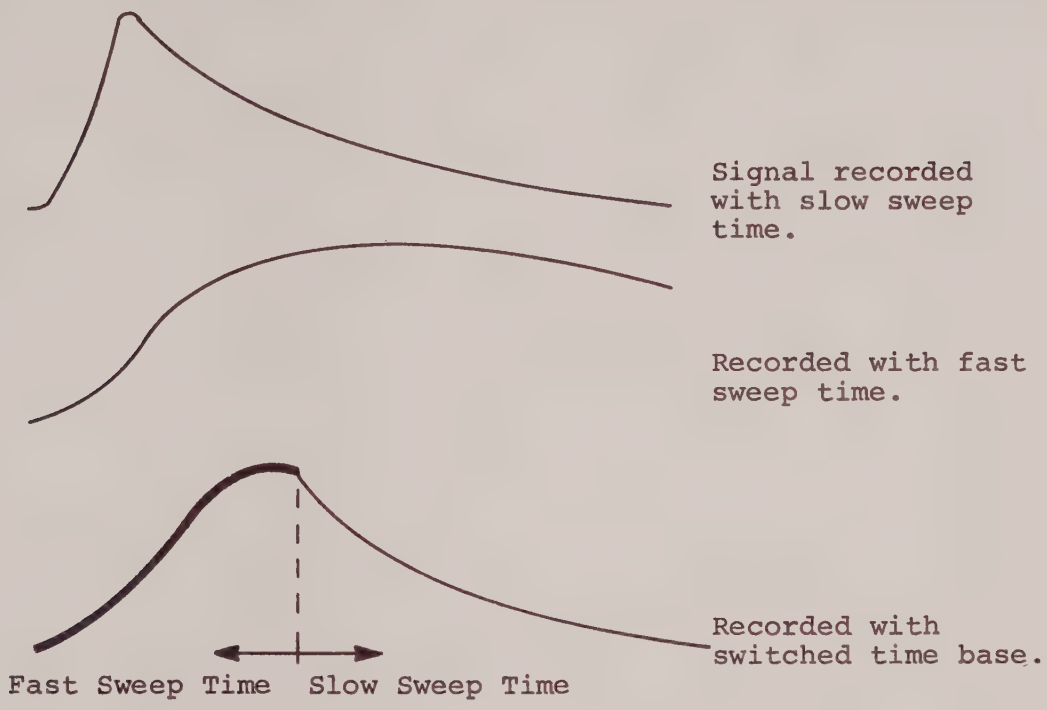


Figure 3.6 Pretrigger Recording.

D. Switched Time Base.

This mode of operation is another unique feature of the Model 802. In this mode an input signal can be stored with portions of the signal recorded at two independent rates. This mode is particularly useful in studying waveforms which contain both a fast and slow time component. The point at which the instrument switches from "Sweep Time A" to "Sweep Time B"

can be adjusted by use of the Delay control. Operation in this mode is illustrated in Figure 3.7.


Signal recorded with slow sweep time.
Recorded with fast sweep time.
Recorded with switched time base.
Fast Sweep Time
Slow Sweep Time

In this mode data is recorded immediately after receipt of a trigger signal with no delays involved.

Figure 3.7

3.5 Limitations

The Model 802 is basically an all-digital instrument. The user should not overlook this fact because, by its very nature, the digital approach to signal storage has certain limitations. There are some conditions under which these limitations can seriously affect the quality of the information stored. This section will deal with these limitations.

There are four basic limitations in using the Model 802 to store electrical transients. The four limitations will be dealt with separately in the discussion that follows.

A. Sampling Rate

The sampling theorum states that the sampling rate must be at least twice the highest input frequency to be measured. In practical situations any complex waveform, such as a sine wave, should have at least five data points throughout the full cycle in order to tell from visual observation some of the signal details. The sampling limitation can easily be demonstrated by taking a high frequency continuous signal, such as a sine wave, and operating the Model 802 through all of its available sweep speeds. It will be observed that at slow sweep speeds a very respectable signal can be obtained which bears little or no relationship to the input signal. This limitation can be avoided by the use of the proper sweep time or with an external low pass filter to limit the high frequency inputs.

B. Output Smoothing

The digital information coming out of the Model 802 memory goes through a smoothing digital-to-analog converter. This converter makes the output appear to be a somewhat continuous trace rather than a series of points normally expected from a digital instrument. The most important point to remember is that the digital information contained in the memory may indicate a better risetime than the visual presentation because of the smoothing circuit employed in obtaining the visual presentation.

C. Amplitude Resolution

The Model 802 converts all analog input signals to an accuracy of 8 binary bits. This means that the resolution can be no better than 1 part in 256, or 0.4% accuracy.

D. Time Resolution

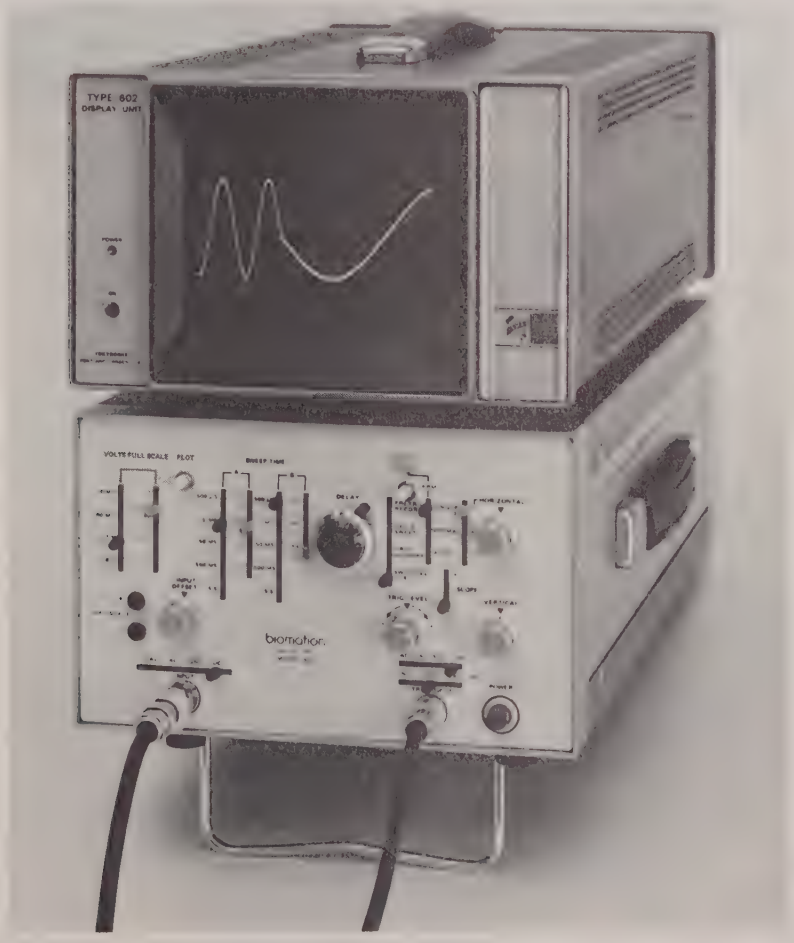
The memory in the Model 802 contains 1024 words of information. Normally only the first 1000 words are used on a CRT display. Any sweep time set on the front panel of the Model 802 corresponds to the use of 1000 words of information. This means that when using a sweep time of 500 μsec, for example, a new point is stored in memory every 0.5 μsec (500 μsec ÷ 1000). The time limitation is directly related to the sampling rate limitation described in Item A above.

SECTION IV

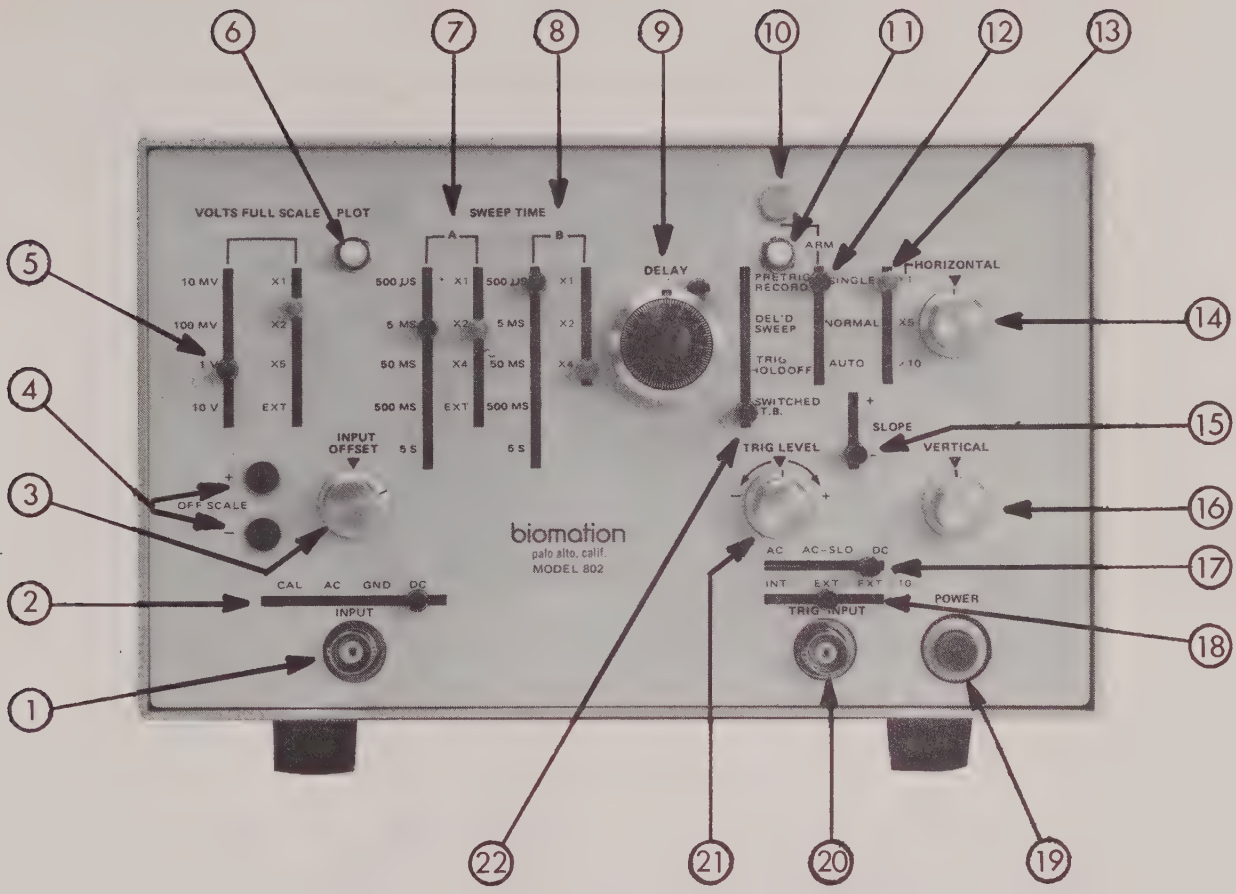
Operation

4.1 Introduction

Front panel controls, rear panel connections and typical operating procedures are covered in this section. The purpose of this section is to assist the user in the proper operation of the Model 802. Items to be discussed are a complete description of the front panel controls and their effective ranges, location and proper use of rear panel connectors, setup procedures prior to using the Model 802, and step-by-step operating procedures in each of the four modes of operation. After completion of this section the user will have gained knowledge and confidence in the proper use of the Model 802.



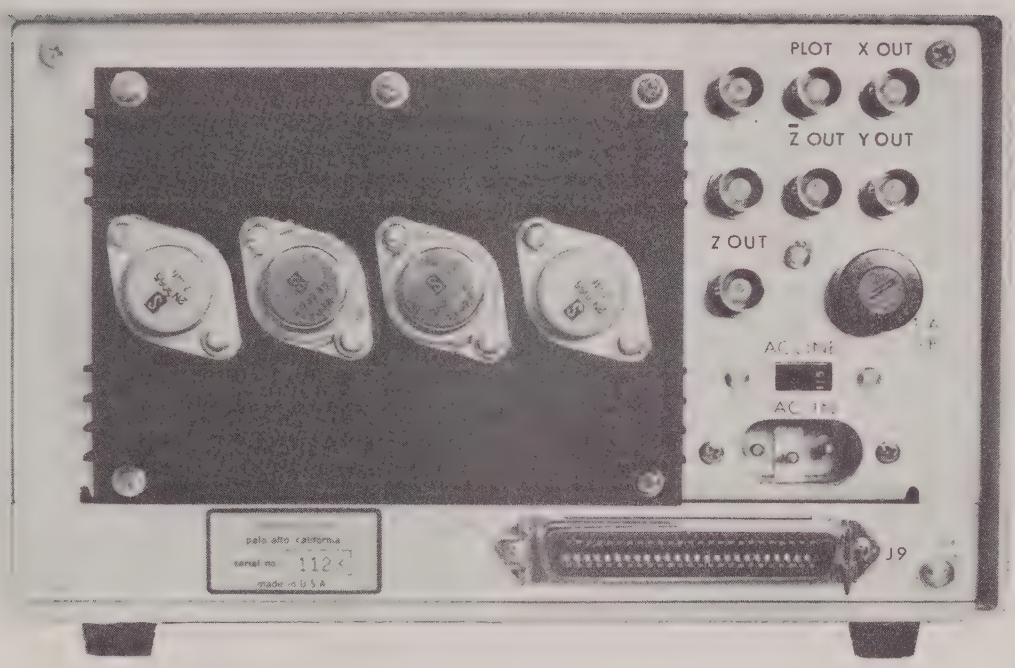
The above photo shows the Biomation Model 802 Transient Recorder interfaced with a commonly used output device.



4.2 Front Panel Controls

1.	Signal Input Connector	Impedance 1 megohm ‖50 pf.
2.	Input Switch	Provides selection of DC coupling, AC coupling, ground and calibration signal.
3.	Input Offset Control	DC input level compensation + or -1.5 times input range.
4.	Offscale Indicators	Indicates ADC saturation.
5.	Volts Full Scale	Adjusts input sensitivity of amplifier from 10 mV to 50 V.
6.	Plot Pushbutton	Initiates plot output when trigger select (12) is in Single.
7.	Sweep Time A	Selects sweep time to record 1000 points of data.
8.	Sweep Time B	Selects sweep time during B portion of Switch Time Base mode.
9.	Delay	Controls amount of delay introduced in trigger circuits in Pretrigger Record Delayed Sweep and Trigger Holdoff mode. Determines changeover point in Switched Time Base mode.
10.	Arm	Indicates when trigger circuit is ready to accept new trigger.
11.	Arm Pushbutton	Arms trigger circuit when trigger selector is in Single.
12.	Trigger Mode Select	Selects Single, Normal or Auto triggering modes.
13.	Horizontal X	Selects horizontal expansion X1, X5 or X10.
14.	Horizontal Position	Adjusts DC offset on X ramp for X-Y CRT displays.
15.	Slope	Selects trigger slope + or -.
16.	Vertical	Adjusts DC offset on the Y output for CRT and recorders.
17.	AC-AC Slo-DC	Selects trigger input coupling networks.
18.	INT-EXT	Selects trigger source internal, external or ÷10.
19.	Power	On/off switch and pilot lamp.
20.	Trigger Input	External trigger input jack.
21.	Trigger Level	Adjusts trigger level between -5 V and +5 V.
22.	Operating Mode Select	Selects Pretrigger, Delayed Sweep, Trigger Holdoff or Switched Time Base modes of operation.

NOTE: For proper operation, the slide switch knobs must be in the mechanical detent adjacent to the function designation.



4.3 Rear Panel Connectors

Plot Out	Y output to a plotter or strip chart recorder. Normally 0 V, follows Y during "plot".
X Out	2 msec ramp output for driving X-Y display output 1 V - X1, 5 V - X2, 10 V - X10 with offset.
$\overline{Z}$ Out	32 µsec wide pulse from -10 V to 0 V for retrace blanking or oscilloscope trigger.
Y Out	1 V p-p full scale signal to Y input of X-Y display or vertical input of oscilloscope with offset.
Z Out	32 µsec wide pulse from +10 V to 0 V for retrace blanking or oscilloscope trigger.
Fuse	1 amp slow blow fuse for 115 V (0.5 amp fuse for 230 V).
115/230	Line voltage selector switch.
AC Line In	Power line connection for instrument, 100 watts. Mating power cord Belden #17358.
Connector J9	Digital outputs and commands. See Output Interface Section 5.7 for pin-out and specifications.

4.4 Set-up Procedure

The next step in the operation of the Model 802 is the set-up. To accomplish this, connect the power cord to the power receptacle on the rear panel. Check the voltage selector switch and set it to the proper line voltage, 115 or 230. Then connect the power cord to the power outlet.

The next step is to interface the Model 802 to some type of output device. In this section we will use an oscilloscope. For other interfaces see Section V of this manual, Output Interface.

Connect the Model 802 to the oscilloscope as shown in Figure 4.3.

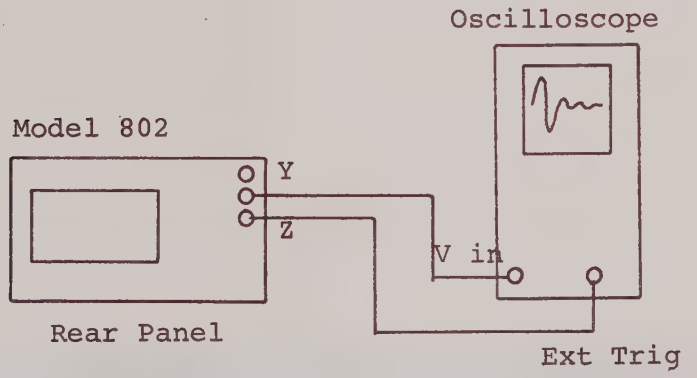


Figure 4.3

Turn on both instruments and allow them to warm up approximately 10 minutes. Set up the oscilloscope as follows:

Vertical Sensitivity	.2 V/cm DC coupled
Vertical Position	Mid-range
Horizontal Sweep	.2 msec/cm
Trigger	Normal
Slope	+
Trigger Input	External DC coupled

Set up the Model 802 controls as follows:

Input Switch	CAL
Input Offset	Mid-range
Volts Full Scale	10 mV X2
Sweep Time A	5 msec X1
Delay	Full CCW "0"
Mode	Trigger Holdoff
Trigger Select	Auto
Slope	+
Trigger Level	Mid-range
Trigger AC-DC	DC
Trigger INT-EXT	EXT
Vertical Position	Mid-range

The waveform on the oscilloscope should be a squarewave as shown in Figure 4.4.

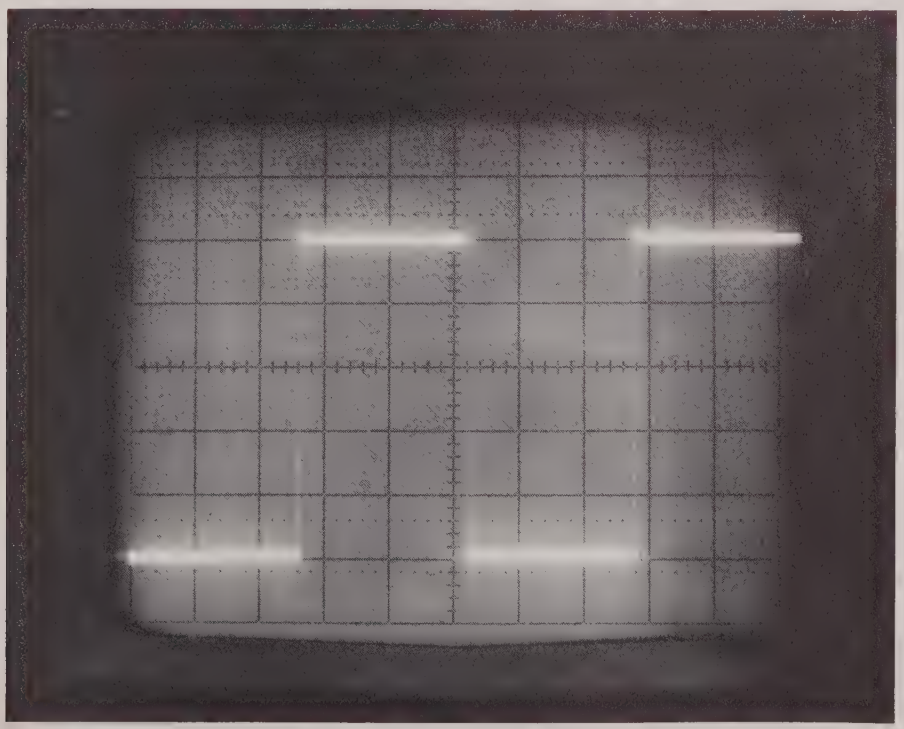


Figure 4.4

Some adjustment of the Model 802 Vertical Position controls may be necessary to center the waveform on the oscilloscope CRT. Also adjust the Input Offset control so that both + and - offscale lights are on. If the waveform is not as shown, recheck all connectors and repeat the set-up procedures before proceding.

4.5 Operating Procedure

In this section of the manual we will operate the Model 802 in all four modes. Although all of these modes may not be of interest to you, we recommend that the procedure be followed as a performance check of the instrument. Some additional equipment will be necessary for operation in this section. They are: a function generator capable of sine, ramp and triangular waveforms at frequencies from 0.01 Hz to 100 kHz; a pulse generator capable of fast rise pulses, with single pulse capability.

4.51 Trigger Holdoff Mode

This mode of operation was used during the previous set-up procedure. However, the Delay control was set at minimum.

Connect the output of the function generator to the input jack of the Model 802. Set the input selector to "DC". Set the Volts Full Scale to 1 V X5. Adjust the generator output for a 5 V p-p output.

Set the Model 802 controls as follows:

Input Selector	DC
Volts Full Scale	1 V X5
Sweep Time	5 msec X1
Delay	Full CCW "0"
Mode Select	Trigger Holdoff
Trigger Select	Normal
Slope	+
Trigger Level	Mid-range
Trigger INT-EXT	INT

Set the function generator controls as follows:

Sine Wave Output	
Output Frequency	200 Hz

Display should be a sine wave. Some adjustment of input offset control may be necessary to center wave. Generator output may also have to be adjusted, increase to obtain full scale or reduce to eliminate clipping of top and bottom of waveform.

Once a satisfactory display is obtained, begin rotating Delay control clockwise. As this control is rotated, the display should start to flicker slightly. This is due to the action of the Trigger Holdoff in that more display time is present between record cycles. The delay time is preventing new trigger signals from being accepted by the trigger circuit. Now rotate the Delay control back to minimum.

4.52 Delayed Sweep Mode

The setup for this mode will be the same as for the Trigger Holdoff mode except move the mode selector switch to "Delayed Sweep". Again a sine wave should be on the display. Now rotate the Delay countrol clockwise. As this is rotated the sine wave should appear to move to the left and as the control is advanced further, the sine wave will continue to appear to move until a total of 10 have passed from right to left. This is because we are actually triggering on the first available signal but recording what occurs up to 10 times the sweep speed later in time. Since the period of one sine wave is the same as the sweep time, 10 cycles have passed before the recording took place.

Return the Delay control to its full CCW position.

4.53 Switched Time Base

The setup for this mode is the same as the previous two modes except: set the mode selector to "Switched T.B."; set Sweep Time B to 5 msec X2. With the Delay control set to minimum, all of the record time is at the rate set by the "B" sweep time. Two complete cycles of the waveform should be observed on the display. As Delay is increased, more of the record time will be at the "A" sweep rate. Typically the Delay control will have to be set to the 1.00 position before any time is recorded at the sweep time A rate. Rotate the Delay control until one-half cycle of "A" sweep time and one complete cycle of "B" is recorded. Advance the Delay control until all of the record time is at the "A" sweep rate. Now return the Delay control to its minimum setting.

4.54 Pretrigger Record

Set up the pulse generator for a 1 msec wide pulse. Set repetition rate for "Manual". Set output level of pulse generator for "positive" and 5 V p-p.

Set up the Model 802 as follows:

Mode	Pretrigger Record
Delay	Minimum "0" delay
Trigger Select	Single
Slope	+

Connect the pulse generator to the Model 802 input. Press the Arm button. The unit should go out of the display mode. Now press the single pulse button on the pulse generator. The Model 802 should return to the display mode with a straight horizontal line. If the Model 802 does not return to display, check trigger level settings. Advance the Delay control to half of one turn. Arm the Model 802 and press the single pulse button on the pulse generator. The full pulse or a portion of it should be on the right edge of the display screen. Advance the Delay control to one full turn. Arm the Model 802 and press the single pulse button on the pulse generator. The pulse should now be left of center on the display.

The Model 802 is triggering on the positive leading edge of the pulse. Therefore, the time before, during and after the trigger is displayed on the CRT.

SECTION V

Output Interface

5.1 Introduction

The Biomation Model 802 Transient Recorder is basically a digital instrument that operates as if it were a conventional oscilloscope. Full utilization of this instrument is only achieved when it is interfaced properly to an output device. Such analog devices as oscilloscopes, X-Y displays, X-Y plotters and strip chart recorders may be used. The digital outputs can be interfaced to equipment such as high speed digital computers, line printers, digital tape recorders, paper tape punches and similar equipment.

The Model 802 has a 1024 word memory. Each time the instrument is triggered, new data is stored in the memory in the time span set by the Sweep Time controls. In analog display 1008 words of information are displayed, with the last 16 words used for retrace of the CRT system. Therefore, the calibration of the Sweep Time control is for the first 1000 words of memory.

While the input rate of storage can be changed by the Sweep Time controls, the analog output rate is fixed at a 2 μsec/word rate for use with X-Y CRT displays and oscilloscopes. A slow fixed rate output is used for Y-time plotters and strip chart recorders. This rate is a word every 0.1 sec (adjustable by internal jumper). In the digital output mode the data can be taken asynchronously at a 2 to 500 μsec/word rate, or at a rate slower than 2.05 msec/word. The Model 802 provides for external control or sensing of the input amplifier gain, Volts Full Scale and Sweep Time. The digital address of the memory is available at the rear panel connector. A complete call-out of the rear panel connector (J9) is given at the end of this section.

5.2 Analog Interface & System Calibration

For CRT displays the data is clocked out of the memory at a fixed rate of a new word every 2 μsec. Cycle time for full memory content is, therefore, 2048 μsec or 2.048 msec. The Y output has an output of 1 V p-p with a full scale input and the vertical position control provides for a $\pm$1.5 V offset.

The Model 802 provides a synchronous X ramp for horizontal beam deflection in an X-Y display system. The X ramp operates over the first 1008 address locations so that the last 16 addresses are not available for display. The amplitude of the X ramp is 1 V p-p and can be increased to 5 V and 10 V respectively for the X5 and X10 "horizontal" positions. A Z output and its complement are available for CRT blanking in an X-Y display. The Z output is normally at +15 V and goes to 0 V during retrace. In the Switched Time Base mode the Z level changes to +10 V during Enhance (for Time Base B). The $\overline{Z}$ complement is normally at -15 V and goes to 0 V during retrace. In the Switched Time Base mode, $\overline{Z}$ goes to -10 V during Enhance (for Time Base B).

Figure 5.1 shows a timing diagram and the relationship of the X output, Y output, Z and $\overline{Z}$ outputs.

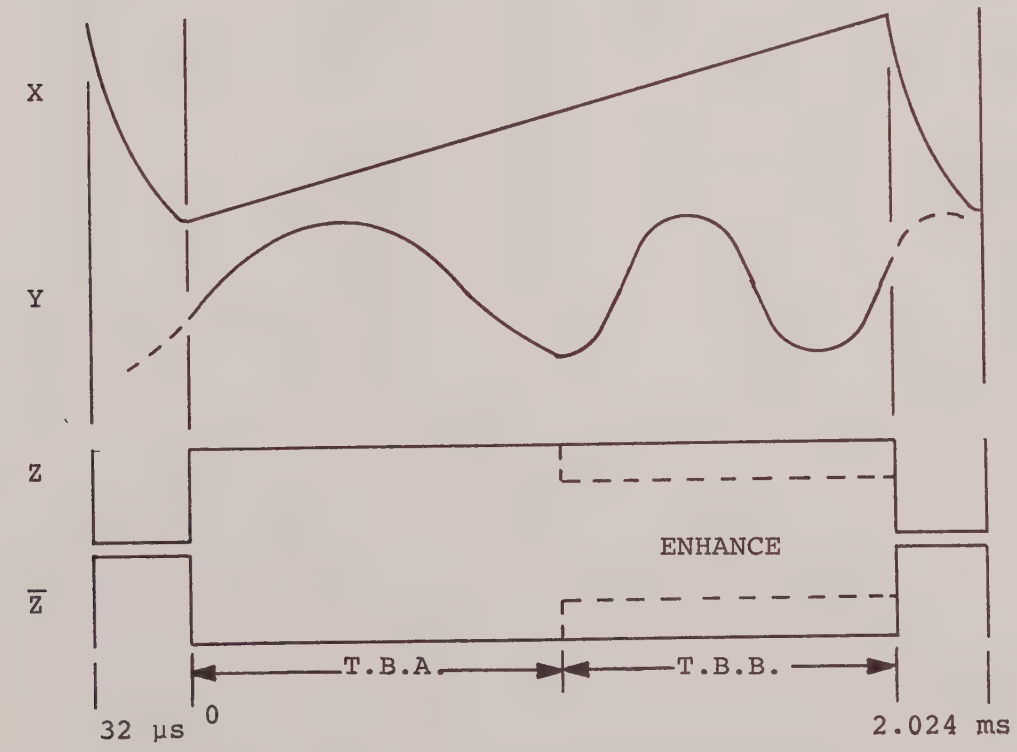


Figure 5.1

5.21 Oscilloscope Interface

Figure 5.2 shows an interconnection between the Model 802 and an oscilloscope using the internal time base of the scope.

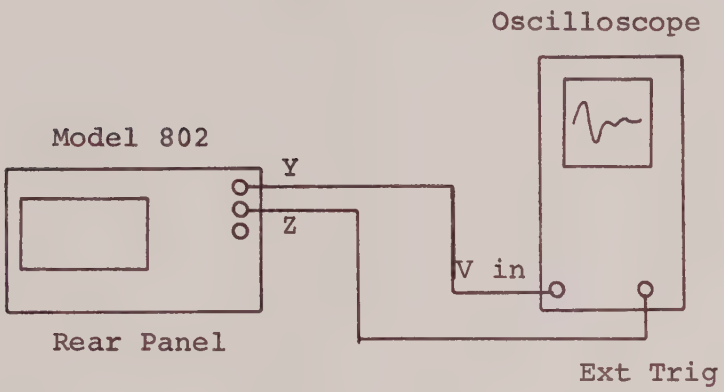


Figure 5.2

The Y output of the Model 802 is connected to the vertical input of the oscilloscope. The V/cm is set to 0.2 V, DC coupled. The Z output of the 802 is connected to the external trigger input of the oscilloscope. Set the sweep speed of the oscilloscope to 0.2 msec per division. Set the slope of the trigger to positive. The Y output of the Model 802 can now be displayed on the oscilloscope.

5.22 X-Y Display

Figure 5.3 shows the connection of the Model 802 to an X-Y display device.

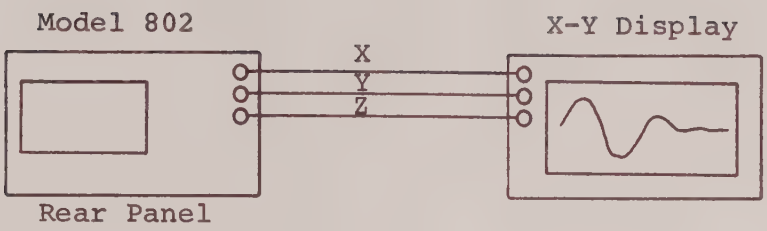


Figure 5.3

Connect the Y output of the Model 802 to the Y input of X-Y display. Connect the X output of the Model 802 to the X input of the display. After a signal has been stored in the 802 and viewed on the display, connect the Z or $\overline{Z}$ outputs to the display, depending on the polarity required by the X-Y display.

5.23 Plotter Interface

The plot output of the Model 802 can either be initiated by pressing the Plot pushbutton located on the front panel, or by grounding pin 8 of J9 located on the rear panel for at least 2.5 msec. The plot command will operate only when the instrument is in the Single Sweep trigger mode. During plot output the Model 802 changes from the high speed display clock rate of 2 μsec/word to a slow speed clock rate of 0.1 sec/word. This output rate will require 102.4 sec for plotting the 1024 words in memory. The plot output is grounded to prevent recorder chatter prior to plot. During the plot operation the plot output signal has the same characteristics as the Y output signal. The output signal has a full scale span of 1 V within the limits of $\pm$1.5 V, as controlled by the vertical position control. The plot output is filtered to provide a smoother trace. A write command is available at the rear panel for use with the plotter. This signal goes high (+4 V) during plot but is otherwise at 0 V.

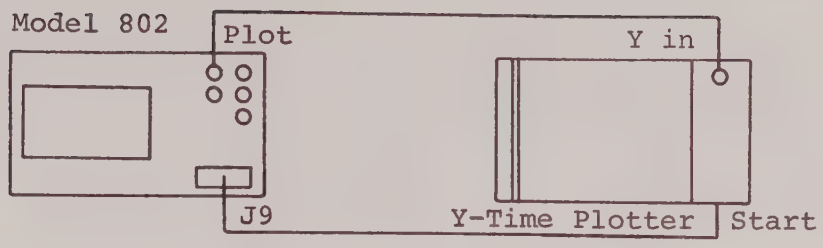


Figure 5.4

Figure 5.4 shows an interconnection diagram for the Model 802 to a Y-time plotter. The Y input sensitivity of the plotter should be set at 0.2 V per major division. A time scale of 10 sec per major division should be set for X. This will produce an output plot in a chart size of 5 x 10 divisions.

5.3 System Calibration

After connecting the Model 802 to either an oscilloscope or an X-Y display, the system should be calibrated to insure that the display will have a calibrated output in both amplitude and time. Set the front panel controls on the Model 802 as follows: Volts Full Scale to 10 mV and X2. Set the input selector switch to Calibrate and adjust the input-offset control so that both the positive and negative offscale lights are on. This setting will produce a full scale output of 1 V to the display. Set the display Y sensitivity so that the square wave stored in the Model 802 occupies 5 div. on the vertical axis. The second transition of the square wave calbrated input occurs at address 512. Adjust the X sensitivity of the display so that this transition occurs exactly 5.2 div. from the far left graticule. You now have a calibrated system of the Model 802 and the display device in both amplitude and time. This calibration is constant for all sweep speeds and input Volts Full Scale settings. Once this calibration has been performed, the X and Y sensitivities of the display device should not be changed.

5.4 Digital Interface

The timing diagram for the digital interface is shown in Figure 5.5. The signals involved are available at the rear panel connector J9. These signals are individually described later and in all cases the levels are compatible with TTL or DTL logic circuits. In referring to the "high" and "low" levels, signals are +3 to +5 V and 0 to +1 V respectively.

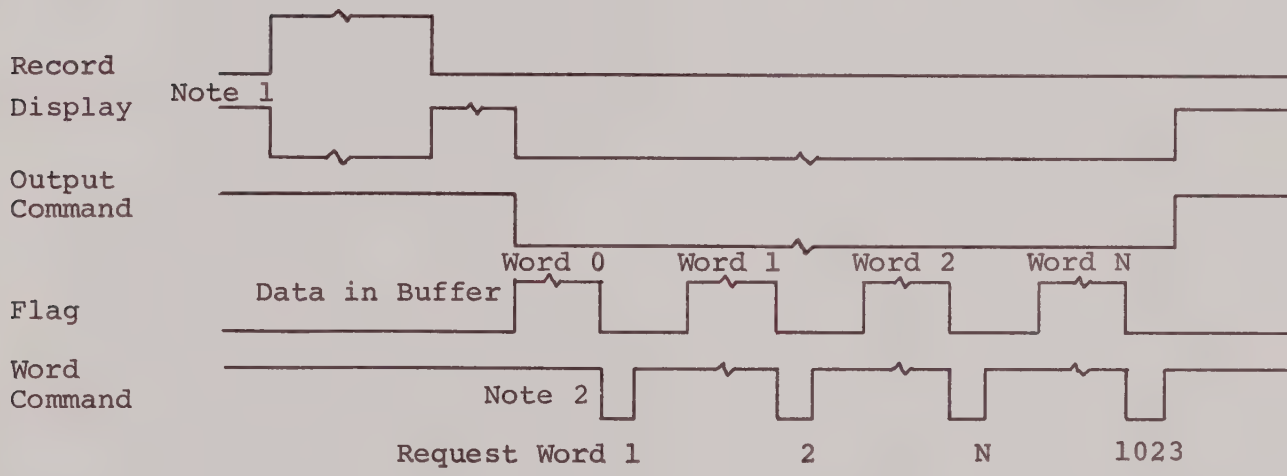


Figure 5.5

Note 1. Not available at rear panel.

Note 2. Digital output always starts at the fast rate. If a delay of more than 500 μsec occurs between command pulses, all further points will have 2 msec latency.

5.41 Data Format

The Y digital data format is 8 lines parallel binary, positive true (+3 V true, 0 V false). The X (memory location) data format is 10 lines parallel binary, positive true (+3 V true, 0 V false).

5.42 Data Availability

The digital output data is available any time after a record cycle has been completed by the Model 802. The output command will only operate when the unit is in the Single Sweep mode of operation. The analog equivalent of the stored signal may be viewed for any period of time before the digital data is taken. The digital data may be taken as many times as the user wishes. The output routine is entered by grounding pin 7 of the output connector (J9). The output routine can be exited by raising the output command to its normal high level.

5.43 Data Output Rates

The data may be taken asynchronously with the memory at a rate of 2 µsec to 500 µsec without any latency or waiting time for the memory to completely recycle. The data may also be taken asynchronously at rates of 2.05 msec or slower. The data cannot be taken at rates between 500 µsec and 2.05 msec. The system may be operated in an interlock or non-interlock mode. In the interlocked mode of operation the negative transition of the Flag is used to take away the Word Command input. In a non-interlocked mode of operation a 0.5 µsec wide negative going pulse is used to initiate the Word Command cycle. The Flag output line will go high when the data is in the output buffer. It will remain high until the next Word Command is received, at which time it will go low. It will stay low until the next word of inforamtion is in the output buffer. Flag should be used as a data strobe by the output device.

5.44 Output Control Sequence

1. The output mode is initiated when pin 7 of J9 is grounded by the output device. This line must be held at 0 V until the output operation is complete. The Model 802 must be operated in the Single Sweep mode.

2. After a latency of up to 2.05 msec, the Flag line will go high (≈4 V) indicating that the first data word is available on the output lines. The positive transition of Flag can be used by the output device to "load" the data into that device.

3. The next word is requested by the output device by supplying a pulse (500 nsec minimum) of +5 V to 0 V to the Word Command input on pin 32 of J9. The leading edge of this pulse will cause Flag to return to 0 V. Flag will return when the next data is available on the output lines. As long as successive Word Commands occur within 500 µsec, the data will appear within about 500 nsec of the Word Command. If longer than 500 µsec lapses between any two Word Command signals, a latency of up to 2.05 msec will occur between the command and data available (Flag). In any case, the Flag will always indicate by its positive transition when the next data is available.

4. Word Command should be continued until Output Mode, pin 42 of J9, returns to 0 V or until sufficient information has been processed. At this time the output pin 7 line should be raised to +5 V.

5.5 Remote Programming & Sensing

The Model 802 provides the user with a capability to either remotely "program" or "sense" the positioning of the Input Sensitivity and the Sweep Time controls. The control lines are available at the rear panel connector J9. In order to program these lines, they must be driven with at least +4 V from a source impedance of no more than 500 ohms. You can also utilize the remote lines to sense the positioning of the controls. The input impedance of the sensing circuit should be no lower than 1 K ohm and able to detect a level of no more than 2 V positive. In order to remotely program the Volts Full Scale and Sweep Time, the switches must be placed in the EXT position on the front panel. The X4 position of the Sweep Time is not brought out to the rear panel but is externally sensed or controlled by its equivalent, which is $\overline{X1}$ and $\overline{X2}$. The memory address counter is also brought out to the rear panel. These lines are for sensing only and are in binary positive true format. They are used to indicate the address of the memory as the data is being output.

Remote program sequence:

1. Place front panel controls to EXT. If Volts Full Scale is in external J9 pin 26, EXT V will go to +15 V. If Sweep Time A is in external J9 pin 28, EXT T will go to +5 V.

2. Drive the proper lines with +4 V.

3. When driving the Sweep Time lines, "Ext T Gate", J9 pin 29 must be grounded.

5.6 External Time Base

An external time base can also be used for the Model 802 sweep time. This is accomplished by placing the front panel Sweep Time control in the EXT position and pulsing the EXT T.B. input J9 pin 30 with a pulse 0.5 µsec wide from +3 V to 0 V. The repetition rate of these pulses must be from 2 µsec to 500 µsec, or 2 msec or slower. The instrument will not function properly when the repetition rate is between 500 µsec to 2 msec.

5.7 Rear Panel Signals, J9 Connector

Mating connector, Amphenol #57-30500

Pin	Signal Name	Description
40	$Y2^0$	Y digital output LSB - 2^0
39	$Y2^1$	Y digital output 2^1
38	$Y2^2$	Y digital output 2^2
37	$Y2^3$	Y digital output 2^3
36	$Y2^4$	Y digital output 2^4
35	$Y2^5$	Y digital output 2^5
34	$Y2^6$	Y digital output 2^6
33	$Y2^7$	Y digital output MSB - 2^7
10	$X2^0$	X digital output LSB - 2^0
12	$X2^1$	X digital output 2^1
13	$X2^2$	X digital output 2^2
11	$X2^3$	X digital output 2^3
14	$X2^4$	X digital output 2^4
16	$X2^5$	X digital output 2^5
17	$X2^6$	X digital output 2^6
15	$X2^7$	X digital output 2^7
18	$X2^8$	X digital output 2^8
19	$X2^9$	X digital output MSB - 2^9
50	X1T	Sweep Time X1 sweep time
47	X2T	Sweep Time X2 $X4 = \overline{X1 + X2}$
44	500 µs	Sweep Time 500 µsec full scale
46	5 ms	Sweep Time 5 msec full scale
48	50 ms	Sweep Time 50 msec full scale
45	500 ms	Sweep Time 500 msec full scale
49	5 sec	Sweep Time 5 sec full scale

Pin	Signal Name	Description
24	X1V	Volts Full Scale X1
25	X2V	Volts Full Scale X2, X5 = $\overline{X1 + X2}$
23	10 V	Volts Full Scale, 10 volt range
22	1 V	Volts Full Scale, 1 volt range
21	100 mV	Volts Full Scale, 100 mV range
20	10 mV	Volts Full Scale, 10 mV range

The above Sweep Time and Volts Full Scale signals can be "sensed" or, with front panel control in "EXT", can be driven by +5 V.

28	EXT.T	External Time signal can be used as an indication from the front panel that the Sweep control is in External.
26	EXT.V	External Volts signal can be used as an indication from the front panel that the Volts Full Scale control is in External.
29	EXT.T GATE	This signal, when held at ground, sets internal logic so the sweep time remote lines can be driven.
30	EXT.T.B.	External Time Base signal can be used to record data at a rate generated by an external source. Pulses should be 0.5 µsec wide from +3 to 0 V. Maximum repetition rate 2 µsec.
7	Output Control	An input which, when grounded, stops the normal display and initiates the digital output of data.
32	Word Command	This input commands the successive digital words during output. Pulse should be normally +3 and go to 0 V for 0.5 µsec.
31	Flag	The Flag output indicates new data available in the output buffer when it makes a transition from 0 V to +3 V. It goes low upon receiving the next word command from pin 32.

Pin	Signal Name	Description
8	Plot P.B.	An input, when grounded for 2.5 msec, initiates the plot output mode.
9	Remote Arm	Arms the trigger circuits. Arming is obtained with a pulse from +3 V to 0 V with a width of 0.5 to 1 µsec.
43	Digital Trigger	Triggers the instrument from an external digital command rather than an input signal. Trigger is initiated with a pulse from +3 V to 0 V with a width of 0.5 to 1 µsec. Front panel controls must be set as follows: Slope - Trigger Input EXT Level Full -
6	Z Enhance	An output used with the X digital signals which indicates at what point the time base switched speeds in the Switched Time Base mode of operation. Signal normally at 0 V goes to +3 V at switch point.
41	Plot-out	This output goes to +3 V from 0 V. During Plot output it can be used as a pen lift or plot command to an X-Y plotter.
1	GND	Internal ground.
42	Output Mode	Signal level changes from 0 V to +4 V when the Model 802 is in the Output Mode.

CALIBRATION PROCEDURE

6.1 Introduction

This calibration procedure is designed for use by users who are equipped to do in-house calibration and maintenance of their equipment on a routine basis. The Model 802 has been completely tested and calibrated before shipment and a re-calibration should not be necessary for some time.

6.2 Required Test Equipment

The following test equipment is recommended for calibration and service of the Model 802.

Function Generator capable of fast rise time square waves and triangle or ramp outputs.

Voltmeter, 0 to 50 V DC, AC.

Oscilloscope, DC to 50 MHz, dual channel.

Frequency Counter, 20 Hz to 10 MHz.

6.3 Setup Procedure

Assemble the above listed test equipment. Turn on the test equipment and the Model 802 and allow them to warm up for about 10 minutes. Remove the top cover from the Model 802 by removing four screws (2 on each side).

6.4 Power Supply

There are four test points and a grount point located on the upper edge of the power supply circuit board. The power supply voltage outputs are measured at these points and referenced to the ground at the left of C5. The following are the output voltages and tolerances.

Test Point	Voltage	Tolerance	Adjustment
Above C5	+15.00 V	± .04 V	R1
Above C6	-15.00 V	± .04 V	R3
Above C7	-5.00 V	± .15 V	none
Above C8	+5.00 V	± .10 V	none

6.5 Input Amplifier

Turn off power and place input amplifier board on the card extender provided.
Turn power back on.
Set input selector to GND.
Set input offset to mid range.
Connect oscilloscope vertical input to the right lead of R64.
Set vertical sensitivity to 1 V/div.
Set horizontal sweep speed to 0.1 ms/div. Auto trigger.
Set Volts Full Scale as follows: 10 V and X5.
Set vertical position control on scope to a convenient reference line.
Move multiplier to X1 (if trace moves more than 0.2 div., readjust R7 until trace returns to reference line).
Move multiplier switch through its full range. The trace should not move from the reference line. If it does, repeat the above procedure.
Connect the Function Generator output to the input of the Model 802 and set up as follows:
Output frequency 1 kHz square wave.
Set output level to 10 V p-p.
Set 802 as follows: 10 V, X1.
Set input selector to DC.
Adjust vertical position control on scope so that waveform is in a convenient viewing position.
Adjust input offset so waveform is not clipped on the top or bottom.
Figure 6.1 shows the output of the amplifier as it should look. Figures 6.2 and 6.3 show the waveform with abnormal overshoot and rolloff which would require some adjustment.

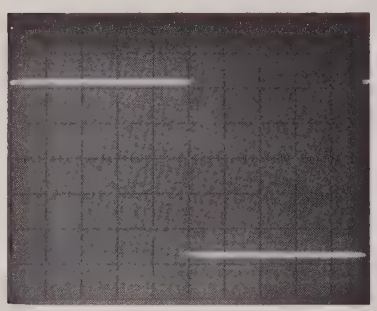


Figure 6.1

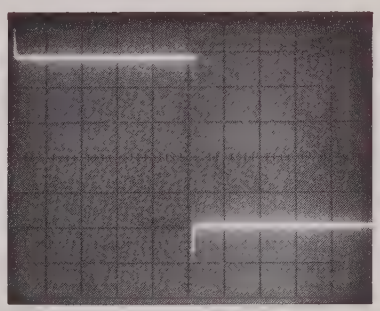


Figure 6.2

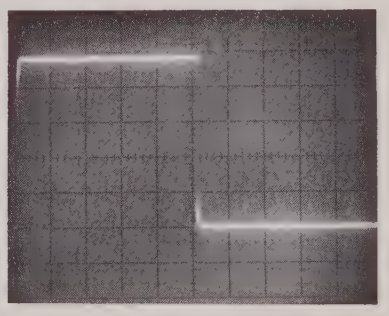


Figure 6.3

If the waveform is not correct, readjust capacitor C19 until it looks like the waveform shown in Figure 6.1. Change the output level of the Function Generator to 1 V p-p. Set the Volts Full Scale controls to 1 V, X1. The output should look like the waveform in Figure 6.4. If it does not, readjust capacitor C17.

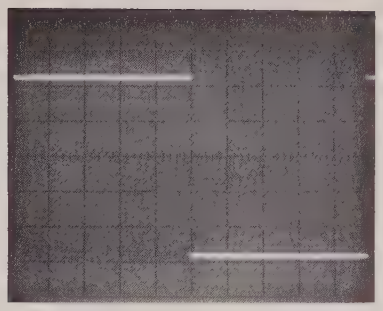


Figure 6.4

Set output of Function Generator to 100 mV.
Set Volts Full Scale to 100 mV, X1.
The output should look like Figure 6.5. If it does not, re-adjust capacitor C15.

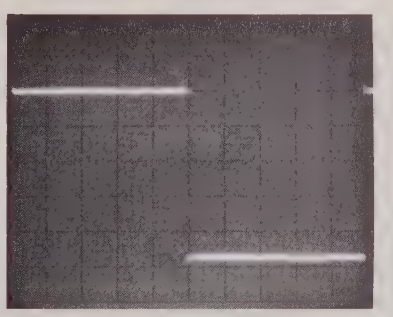


Figure 6.5

Set output level of Function Generator to 1 V p-p.
Set Volts Full Scale to 1 V, X1.
Set horizontal sweep on oscilloscope to 0.5 µs/div.
Risetime of output should be 0.5 µs between 10-90% (as shown in Figure 6.6). If it is not 0.5 µs, readjust capacitors C23 and C22.

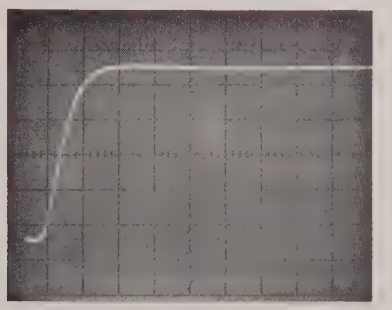


Figure 6.6

6.6 Analog-to-Digital Converter

As described in the circuit description section of this manual, the analog-to-digital converter is divided into two sections. Each section provides 4 bits of the total 8 bits of digital number. Both sections of the converter must operate together for the proper conversion of a signal input.

6.61 First Rank Converter

The voltage levels between the discrimination adjacent points are nominally .300 V. The test points for these levels are the wipers of the potentiometers. The levels are set in the following manner: The first pot in the string (R2) is set to .300 V referenced to ground. The voltage probes are placed with one on the wiper of R3 and the other on the wiper of R4, continuing up the string until all the pots have been set. Figure 6.7 shows a rear view of the first rank converter board with the probes in place. The second rank converter has been removed for better viewing.

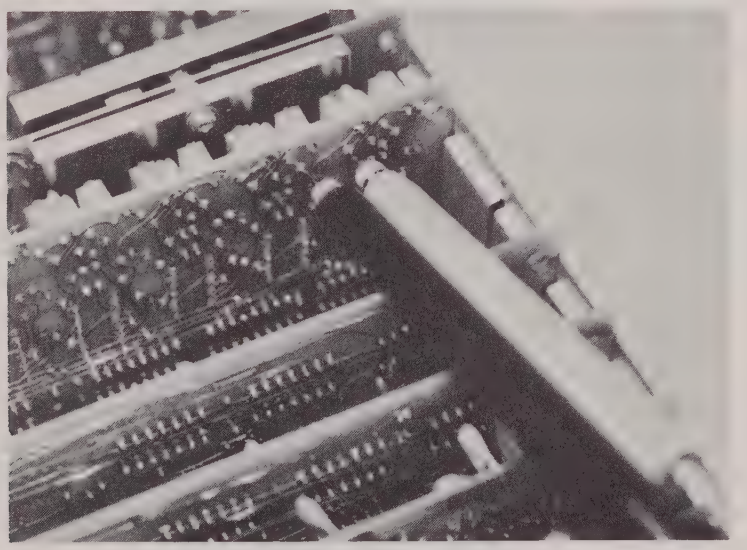


Figure 6.7

It should not be necessary to adjust these potentiometers unless a potentiometer has been replaced.

6.62 Second Rank Converter

The output of the summing amplifier is the resultant of the subtraction of the Summation I and the amplifier output. The dynamic range of the second rank converter is 0 to -4.8 V.

The reference voltages for the converter are divided by resistors R1-R18. Two reference levels are designated on the schematic, V1 and V2. Do not place the second rank converter on the extender card during the following measurements and adjustments because it will effect the adjustment.

Connect the vertical input of the oscilloscope to test point V2.
Set the sensitivity to 1 V/div.
Set the vertical position control to a convenient base line, as shown in Figure 6.8.

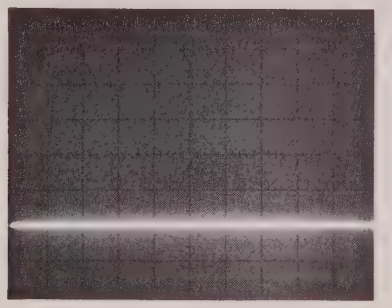


Figure 6.8

Once the base line is set, the vertical position control of the scope should not be moved. Now move the scope probe to the V2 test point (note the level). The correct level is shown in Figure 6.9.

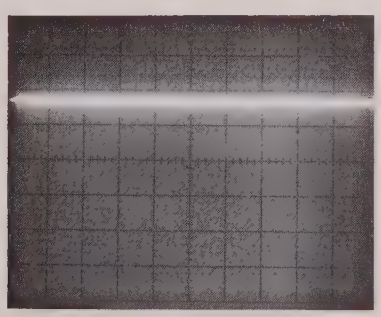


Figure 6.9

Now connect the scope probe to the top of R90.
Set the horizontal sweep speed to 50 µs/div.
Set the Function Generator to a 500 µs ramp output.
Set the trigger control on the Model 802 to EXT.
Place the Mode switch to Pretrigger Record and set the sweep time to 500 µs Xl.
Press the Arm pushbutton.
The waveform should be as shown in Figure 6.10.

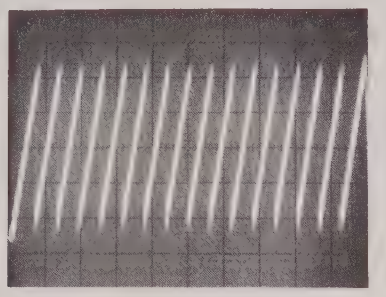


Figure 6.10

If one of the ramps seems to be "out of position", that is, lower in relation to the other ramps, it indicates a drift in settings at the discrimination point in the first rank converter. In this case the potentiometer corresponding to the "out of position" ramp on the first rank converter should be adjusted to bring it in line with the other ramps. Figure 6.11 shows the ramp output of the Model 802 with the second rank converter properly aligned.

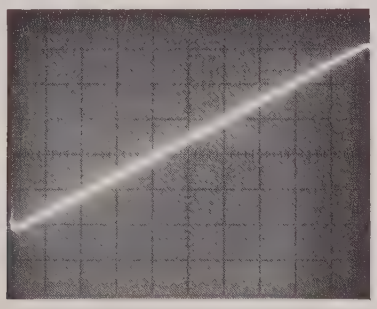


Figure 6.11

The following figures show the effects of three adjustments which are made on the second rank converter. The figure on the left is always the waveform, as seen at the test point, when various controls are out of adjustment. The figure on the right shows what happens to the display.

Figures 6.12 and 6.13 show the effects of R94 (the gain adjustment). In this illustration the gain is set too high. If this control is out of adjustment, the outputs of the two converters will not properly "mesh" and the waveform will appear "lumpy" (as shown in Figure 6.13.

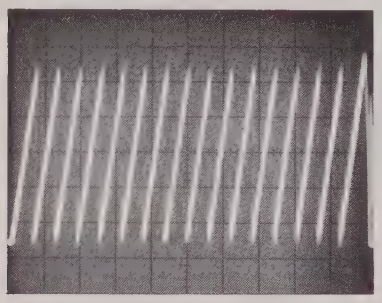


Figure 6.12

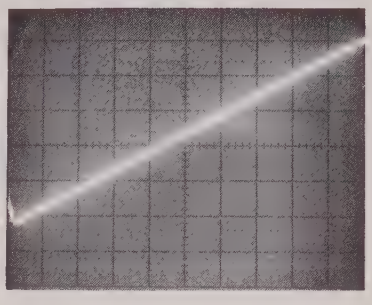


Figure 6.13

Improper adjustment of R102 DC Level Control will cause the output to have a series of 15 steps or notches. Figures 6.14 and 6.15 show what happens when the DC level is set too far positive.

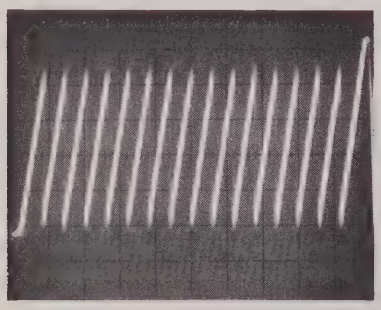


Figure 6.14

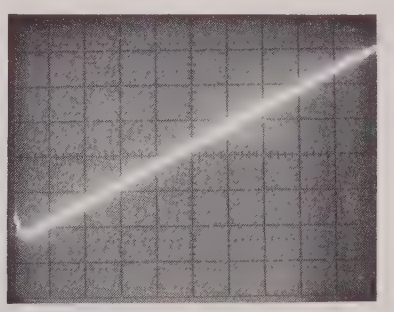


Figure 6.15

There is an interaction between the gain and the level adjustment. Therefore, the two controls must be adjusted in sequence. If the gain control is adjusted, the level control must also be adjusted. This procedure is continued until correct alignment is achieved.

Figures 6.16 and 6.17 show the effects of the zero control R114. If the output waveform has notches on one end but not the other, this usually indicates improper zero adjustment. This control

must be set so that the entire row of ramps is flat and no tilt is present in the waveform.

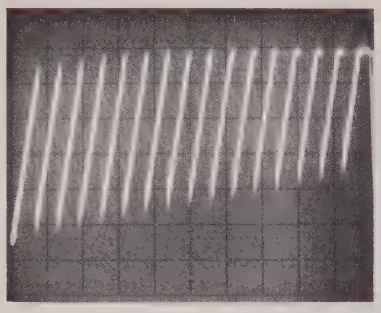


Figure 6.16

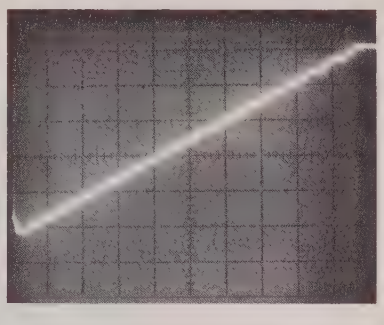


Figure 6.17

6.7 Linear Board Alignment

Three circuits on the linear board may require periodic re-checking and adjustment. The circuits are: the Y digital-to-analog converter, the delay circuit, and the X ramp amplitude adjustment.

6.71 Y DAC

The Y digital-to-analog converter has three adjustments. They are the current supply to the 2^7 bit, current to the 2^6 bit, and the current weight of the three least significant bits. Figure 6.18 shows the output obtained with a ramp input (the Y DAC is properly aligned). Before adjusting the Y DAC, check the analog-to-digital converter for proper alignment.

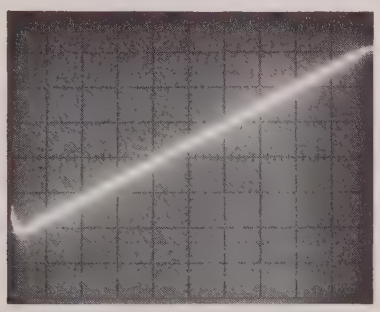


Figure 6.18

Figure 6.19 shows the effects on the output with potentiometer R25 improperly adjusted. The input is still a 500 µsec ramp but the unit is now operated in the Trigger Holdoff mode. The trigger selector is set to single sweep using Internal trigger.

Note that in Figure 6.19 the ramp appears to have two levels with steps at points located 1/4, 1/2 and 3/4 through the ramp. Proper adjustment of R25 will eliminate the steps at the 1/4 and 3/4 points. The step in the center of the waveform will disappear only if R26 ($Y2^7$) is properly adjusted.

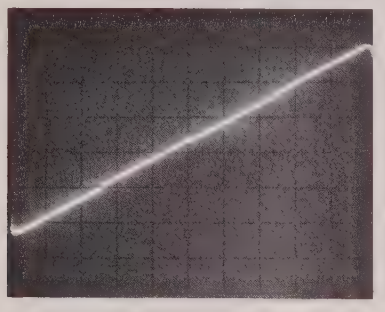


Figure 6.19

Figure 6.20 shows the improper adjustment of R26. Proper adjustment of R26 will eliminate the step in the middle of the waveform.

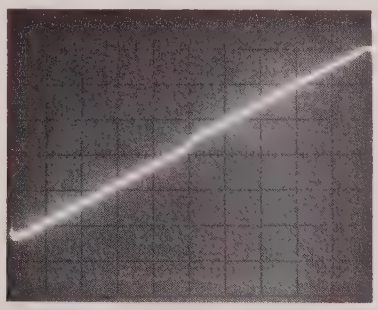


Figure 6.20

The effects of the three least significant bits on the output from the Y DAC is controlled by potentiometer R27. If this control is adjusted improperly so that the current weights of the least significant bits are too small, the output waveform will take on a "lumpy" appearance (as shown in Figure 6.21). If, however, R27 is adjusted so the current weights are too great, the waveform will take on a "shingled" appearance. Proper adjustment of R27 is achieved when the output waveform is smooth and linear.

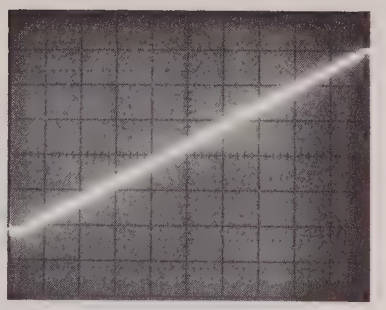


Figure 6.21

6.72 Delay Adjustment

Potentiometer R87 controls the amount of charge that will be placed into the "pump circuit" and thus the amount of delay that will occur. The calibration of the delay control is as follows:

Place the Model 802 in the Delayed Sweep mode.
Place the trigger select to Normal.
Set the Delay control to 5.00.
Set Sweep Time to 5 ms, X1.
Input a 200 Hz triangle waveform.
Set the horizontal sweep of the oscilloscope to 5 ms/div.
Set the trigger to internal, normal, positive slope.
The duration of the positive level (Delay) should be 25 ms.
If it is not, readjust R87 until it is exactly 25 ms.

6.73 X Ramp Calibration

The X ramp is used to drive an XY type oscilloscope or display unit.

Connect the X output of the 802 to the vertical input of the oscilloscope.
Connect the Z output of the 802 to the external trigger input of the oscilloscope. Trigger on the positive slope.
Set gain of oscilloscope to 0.2 V/div.
Set horizontal sweep to 0.2 ms/div.
Set horizontal position control on 802 to mid range.
Set the vertical position on the scope so the start of the trace is on a convenient base line. The start of the trace should be set at the far left Y grid.
Adjust R88 so that the trace intersects at the 10th division on the X axis and exactly 5 divisions above the start of the trace (Y).

Correct adjustment is shown in Figure 6.22. This procedure calibrates the X output to exactly 1 V at 1000 words.

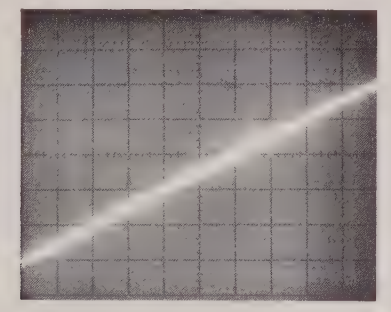


Figure 6.22

6.8 Time Base Frequencies

The following is a list of the time base rates for all sweep speeds.

Front Panel Controls	Rep. Rate	Frequency
500 µs X1 (500 µsec)	.5 µsec	2 MHz
500 µs X2 (1 msec)	1 µsec	1 MHz
500 µs X4 (2 msec)	2 µsec	500 kHz
5 ms X1 (5 msec)	5 µsec	200 kHz
5 ms X2 (10 msec)	10 µsec	100 kHz
5 ms X4 (20 msec)	20 µsec	50 kHz
50 ms X1 (50 msec)	50 µsec	20 kHz
50 ms X2 (100 msec)	.1 msec	10 kHz
50 ms X4 (200 msec)	.2 msec	5 kHz
500 ms X1 (500 msec)	.5 msec	2 kHz
500 ms X2 (1 sec)	1 msec	1 kHz
500 ms X4 (2 sec)	2 µsec	500 kHz
5 s X1 (5 sec)	5 µsec	200 kHz
5 s X2 (10 sec)	10 µsec	100 kHz
5 s X4 (20 sec)	20 µsec	50 kHz

6.9 Disassembly Procedure

The following are disassembly procedures for the Model 802 front panel and power supply sub-assembly.

6.91 Front Panel

Disconnect power cord.
Remove top and bottom covers (4 screws in each).
Remove four #6 hex nuts from inside the front panel (one in each corner).
Use a long 1/4" Spintite for removing the hex nuts.
Gently push the front panel forward out of the unit.

Disconnect the shielded cable (shield connected to the right socket).
Unplug the power switch connector from the mating connector.
Reverse above procedure for re-assembly.

6.92 Power Supply

Disconnect the power cord.
Remove the #4 screws on the top and bottom edge of the heat sink (5 screws).
Grasp the fins of the heat sink and lift gently to disengage circuit board from connector.
Swing bottom edge of power supply out of chassis and remove power supply. If required, separate circuit board from heat sink.
Remove the mounting screws from the four power transistors.
Lift the entire heat sink, with power transistors attached, from circuit board.

6.10 Plot Output Rate Adjustment

The rate at which data is output in the Plot mode is determined by the rate selected on the time base and address board. The factory wired rate is 0.1 sec/word. This rate can be changed, at customer option, by cutting the trace at location "1". Add a jumper wire to the middle pair of holes between "1" and "5" for a 0.2 sec rate. For a 0.5 sec plot rate, place a jumper wire in the "5" location. See Figure 6.23.

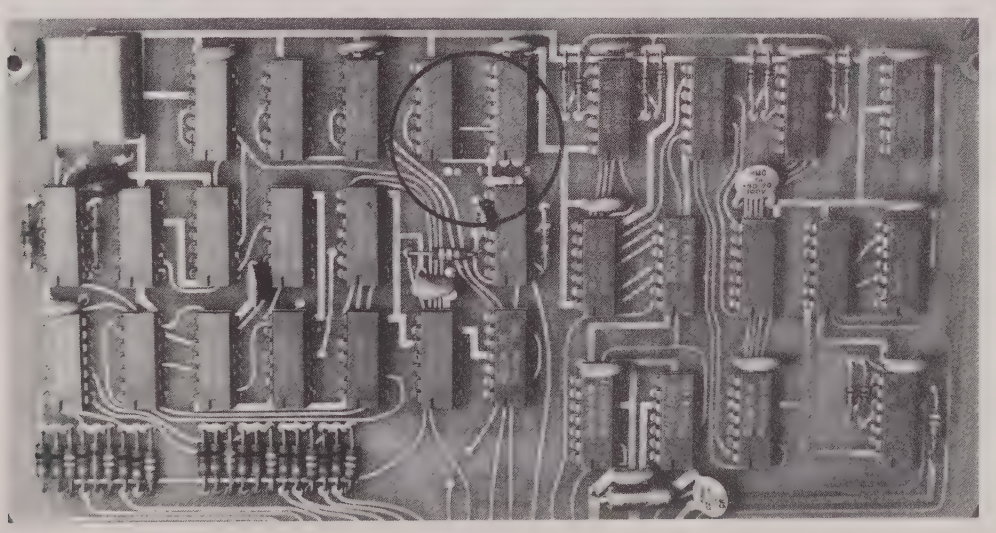


Figure 6.23

The rate can also be increased by a factor of 10 by removing integrated circuit A4. Add a jumper wire from terminal "a" to A5 pin 14.

THEORY OF OPERATION

Using Figure 1 as a reference, the input signal is applied to an attenuator network whose attenuation factor is controlled by the Volts Full Scale selector switch on the front panel. The output of the attenuator is fed to the first stage of the input amplifier. The input amplifier is a non-inverting operational amplifier. The output of the first stage is fed back through a switchable gain control to the input. The gain of the first stage is adjustable from a low factor of 4.2 to a high factor of 22, utilizing reed relays. The output of the first stage is then fed to the second stage amplifier which has a fixed gain of 22. The input offset control's DC level is applied to the input of the second stage. The output of the input amplifier second stage is fed to the first rank analog-to-digital converter. The analog-to-digital converter used in the Model 802 is a dual rank converter. This means that the ADC makes two complete conversions of the analog signal to arrive at the final digital equivalent. As a result, the ADC divides down into two sections on two different circuit boards. Each section of the analog-to-digital converter provides 4 bits of digital information. The digital equivalent of the analog signal is then stored in 8 bit by 1024 word dynamic shift register memory. Once the data is stored in the memory, it is continuously circulated. An output buffer is used to momentarily hold the output words for the Y output used in display. The digital outputs of the output buffer are then fed to a code converter which converts the Gray Code used in the analog-to-digital converter and memory to a binary code. The Y digital outputs are available directly from the code converter. The digital information is then converted back to analog information in the digital-to-analog converter. The output of this DAC is then amplified by the Y output amplifier and also fed to the plot control output.

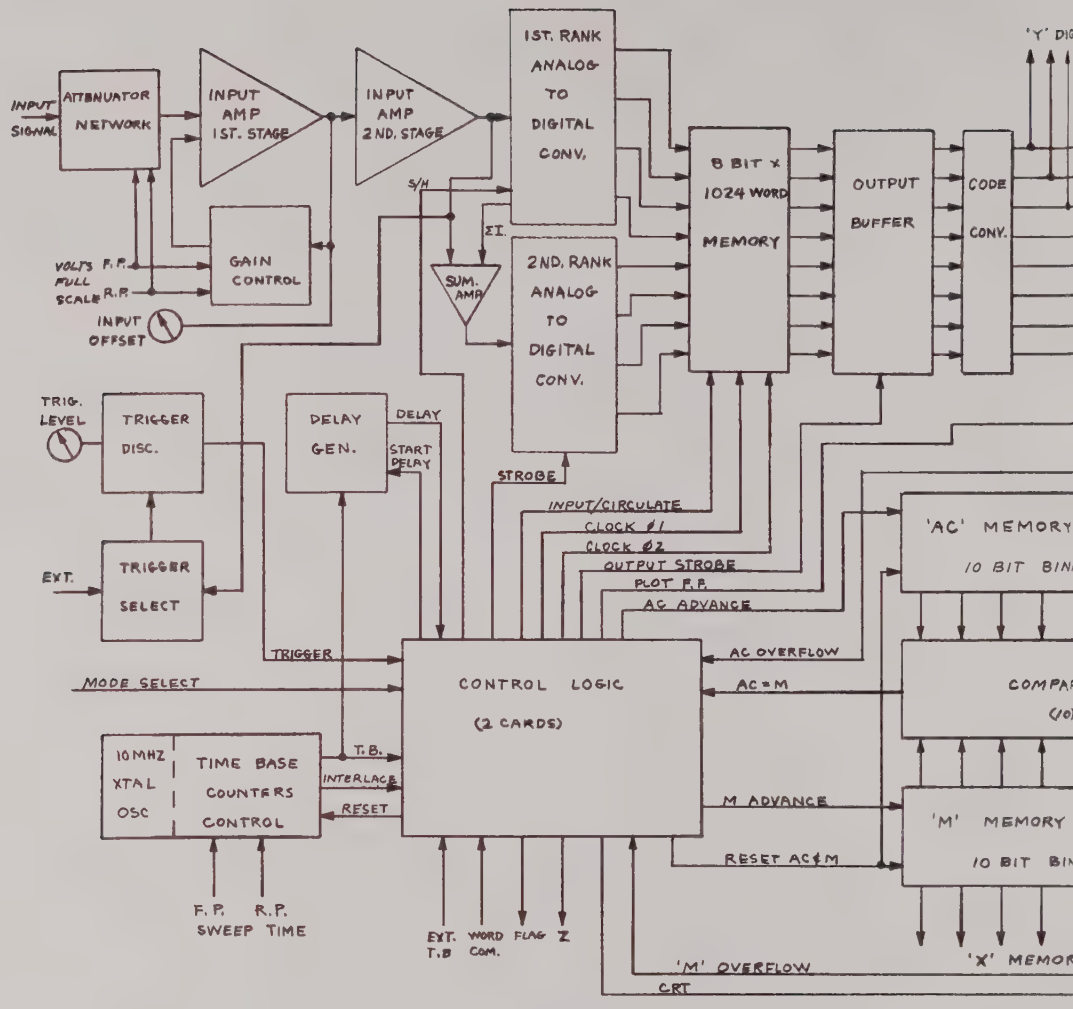
A trigger selection network is provided to select between an externally derived signal or the internal amplifier output signal. The output of the trigger selection network is fed to the trigger discriminator. Here the level of the input signal is compared to a level set by the trigger level control and when the level of the input exceeds that of the trigger level control, a trigger output will be generated to the control logic. When a trigger signal has occurred, the control logic shifts from its normal Display mode into a Record mode. During Record, data is strobed into the output latches of the analog-to-digital converter and into the circulating memory. Two counters, the "AC memory tracking counter" and "M memory tracking counter", keep track of the number of words that have been placed in memory. When these counters count up to 1024 words, an overflow occurs. This overflow is sensed by the control logic and recording of data is ended. The instrument then automatically switches into the Display mode. Here the

data is circulated in the memory and through the output buffer. The output buffer and the memory are strobed at a 2 μsec word rate. The digital data is converted to analog information for presentation on an oscilloscope or XY display. A 10 MHz crystal oscillator and a series of decade dividers are used for time base generation. The rate of the time base is either controlled by the front panel controls or is controlled externally. The time base provides all the necessary clocking control signals for the control logic. The delay generator is used to generate time delays for all four modes of operation. The amount of delay is set by the front panel control labeled "Delay". The control logic provides the signals for the X ramp generation in synchronization with the Y output data and the synchronization pulses for CRT blanking of external devices. The control logic is used during the Output and Plot modes of operation. The control logic generates the flag commands for use in digital data transfer.

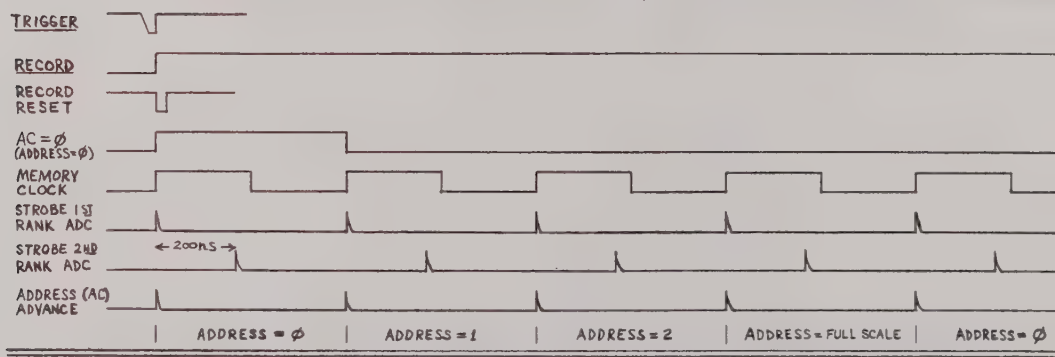
Referring now to Figure 2, Timing Diagram, there are two basic types of recording which take place in the Model 802. One is called "non-interlace". In the non-interlace mode of operation the memory is clocked at the same rate that the data is being strobed out of the analog-to-digital converter. In the interlace mode of operation the memory is clocked at a fast rate and the data is interlaced into the memory as it is circulating. Referring now to the upper timing diagram, non-interlacing, note that the trigger signal initiates the record cycle. Immediately after initiation of a record cycle, a record reset pulse is generated which resets both the AC and M memory tracking counters, the time base, and the memory clock. At the same time, a strobe first rank converter pulse is generated. This pulse transfers the digital data into the quad latch at the output of the analog-to-digital converter. Approximately 200 nsec later a "strobe second rank converter" pulse is generated which strobes the data into the quad latch of the second rank converter. On the negative transition of the clock pulse, data is stored in the memory. At the same time that the strobe first rank pulse was generated, an address advance to the AC counter is generated. Strobe pulses for the first and second rank converter are provided at the repetition rate set by the sweep time controls. The process of storing data into the memory will continue until the AC counter reaches full scale. As soon as AC = 0, a pulse is generated to end the recording of data and the unit returns to the Display mode.

Refer now to the lower timing diagram "Interlace". The interlacing of data into the memory occurs at sweep speeds of 2 sec and slower. In the Interlace mode of operation, a trigger pulse is generated just as before. However, there is up to a 2 msec delay between the trigger pulse and the start of record. This is due to the circulating time of the memory in that the memory address must be at zero before a record cycle is initiated. Once the record cycle is initiated, a record reset pulse is generated which again resets the AC counter, M counter, time

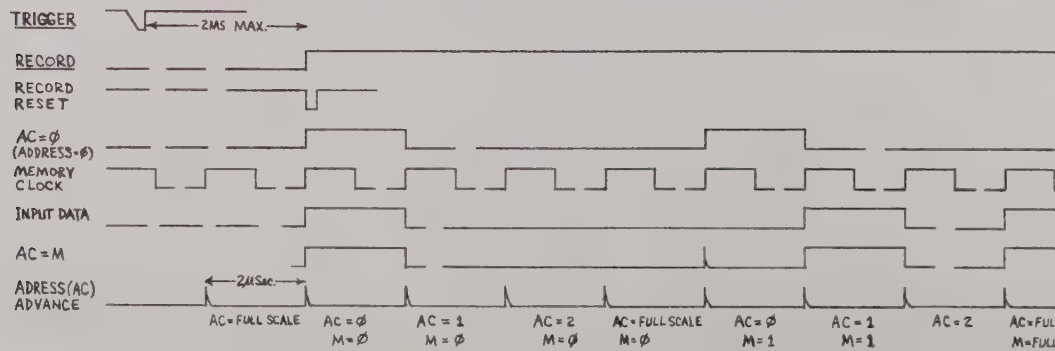
base, and the control logic. In the interlace mode of operation, the memory clock is running at a rate 1000 times faster than the data being input into the memory. The input data line will go true only when AC = M. The M counter is being strobed once every circulation of the AC counter. When the AC counter and the M counter are equal, the first and second rank converters are strobed and the data is entered into the memory on the trailing edge of the memory clock pulse. The "input data" line is then returned to zero and the contents of the memory are circulated until the next AC = M pulse occurs. As the M counter is advanced, the AC = M signal will occur one compartment later in the memory each time the memory is circulated. When the M counter reaches full scale and rolls over, this is sensed by the control logic and the record cycle is ended.



TIMING DIAGRAM / NON-INTERLACE (EXCLUDING PRE-TRIGGER RECORDING



TIMING DIAGRAM/INTERLACE (EXCLUDING PRE-TRIGGER RECORDING)



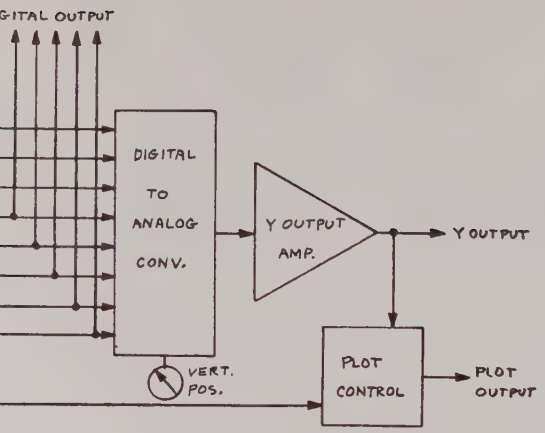
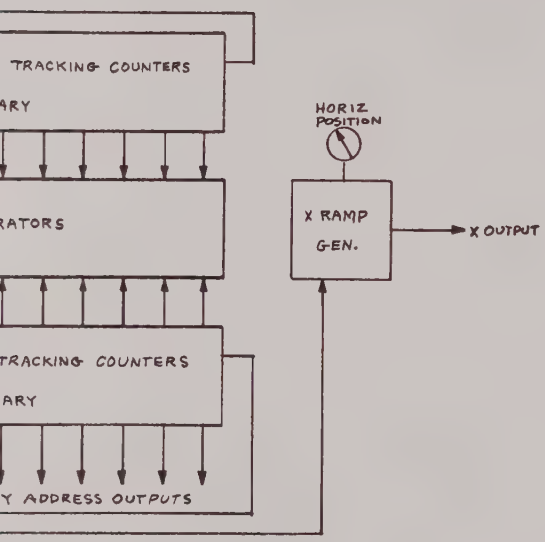


FIGURE 1



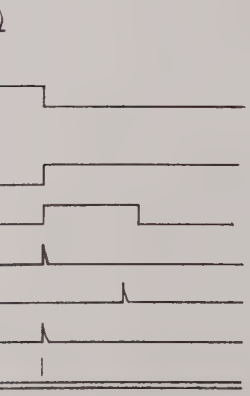
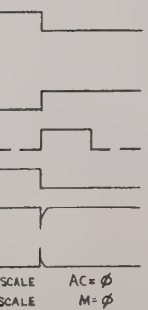


FIGURE 2



THEORY OF OPERATION

Block & Timing Diagram

FRONT PANEL

Introduction

Controls necessary for operation of the Model 802 are conveniently mounted on the front panel. The entire front panel assembly is functional in two respects. The external or front portion of the panel consists of switches, knobs and required lettering for operating the Model 802. The internal or rear portion of the assembly consists of a printed circuit board, circuit components, switch contacts and plug-in contacts which feed the circuits into a central "mother board".

Volts Full Scale

The Volts Full Scale controls are used to control the gain of the input amplifier. Switch S1 selects the range of the input attenuator and switch S2 selects the gain of the amplifier. A voltage level of approximately +5 volts is required to drive the control elements on the input amplifier. This voltage is supplied by the +15 volt power supply dropped through a 2K resistor R1 connected to the wiper of S2. Diodes CR1, 2 and 3 provide a simple "Or" gate to supply power to the wiper of S1. Thus, when S2 is in the external (EXT) position, no control voltages are supplied to the input amplifier. Voltage is then fed to the rear panel connector as an indication to external devices that the front panel controls are in "external". The 50 or X5 position is not brought out to the amplifier.

Plot Pushbutton

The Plot pushbutton is used to initiate the plot output mode. When switch S3 is pushed, this momentarily grounds the input to the control logic and within 2 msec the plot output mode will be initiated. The external plot signal also grounds this same line.

Sweep Time Controls

These controls are used to select the rate at which data will be stored in the instrument's memory. Sweep time A is the main sweep time selector. Sweep time B is used only in the Switched Time Base mode of operation. A voltage of approximately +5 volts is supplied to inputs T1 and T2 by the control logic. A 2K pull-up resistor is used to insure a +5 volt level through CR4 to the wiper of S5. Diodes CR11 and CR9 are connected to S6 and S8 respectively. Diodes CR5, 6 and 7 provide an "Or" gate to supply power to the wiper of S4. You will note that the outputs of S4 and S6 are connected together

through diodes CR8 and 10. The diodes are arranged so that S5 can drive the outputs but S8 cannot provide power to S5 or S4. Inputs T1 and T2 are provided by the control logic to select which time base will be used. When sweep time A is used, T1 is high (+5 V) and T2 is low (0 V), and switches S4 and S5 are active. When sweep time B is used, T1 is low (0 V) and T2 is high (+5 V), and switches S6 and S8 are active. As in Volts Full Scale, the third multiplier position (X4) is not brought out but is determined by the control logic.

Horizontal Expand

This circuit is comprised of a voltage divider for the horizontal ramp output with S16 acting as a selector of the three output levels. The X10 position provides an X output of approximately 10 V p-p, X5 is 5 V p-p, and X1 is 1 V p-p.

Horizontal Position

This control provides a DC level shift to the Horizontal Amplifier located on the linear board and controls the DC offset of the horizontal ramp output. The range of pin W (wiper) is -9.3 V full counterclockwise to +8.8 V clockwise.

Vertical Position

This control provides a DC level to the Vertical Amplifier also located on the linear board and controls the DC offset of the vertical output. The range of pin 20 is 0 V full counterclockwise to -4.4 V full clockwise.

+ and - Offscale Lamps

Lamps designated DS1 and DS2 indicate when a portion of the input signal exceeds the dynamic range of the analog-to-digital converter. They are plug-in cartridge lamps and replaceable from the front. The lamp driver circuits are located on the Control 2 circuit board.

Input Offset

This control provides a DC offset to the second stage of the input amplifier for offsetting a DC level that may be present on the input signal. Normal range of pin C is -5.2 V full counterclockwise to +15.0 V full clockwise.

Delay Control

The Delay Control provides a DC level to the delay generator located on the linear board. During the Switched Time Base mode of operation it is paralleled by a 220 ohm resistor R2 and S11. Normal range is 0 V full counterclockwise (0.00) and +4.9 V full clockwise (10.00). In the Switched Time Base mode the range is 0 V to +1.0 V.

Mode Switch

This switch selects which of the four operating modes will be used. The Pretrigger mode is not brought out but is derived on the control board. Switch S12 is mechanically ganged with S11.

Trigger Mode

Switch S14 selects the triggering mode for the instrument by grounding Single and Auto. Normal is derived by the control logic.

Arm Pushbutton and Arm Lamp

The Arm pushbutton provides a momentary contact closure from which a pulse is generated on Control 1 board to reset the trigger flip-flop. When this flip-flop is reset, the arm lamp will be driven on by the lamp driver.

Input Selector

Input BNC J10 and switch S7 comprise an input selector control for the input amplifier. The outside of J10 is not connected to the system ground until it reaches the input amplifier. This reduces noise on the input. The "Cal" input is a 20 mV p-p square wave used for setup and calibration of the display device.

Trigger Level

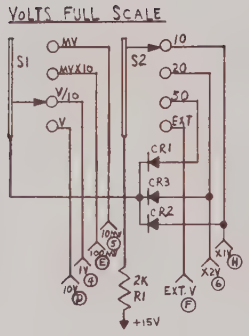
This control provides a DC level to the trigger discriminator located on the linear board. The range at pin S is -3.0 V full counterclockwise to +3.0 V full clockwise.

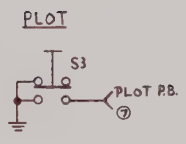
Slope Switch

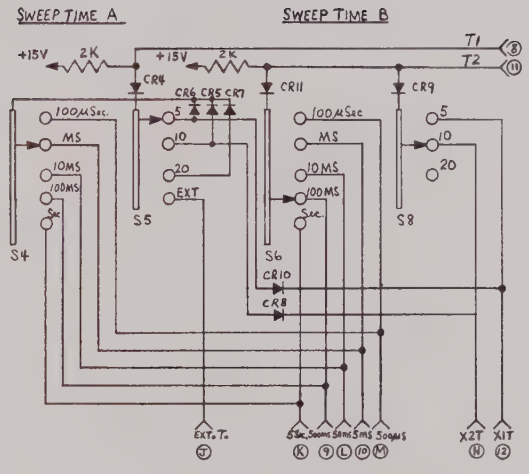
Switch S15 provides a DC level to a logic gate on the linear board to select an inverted or non-inverted signal for the trigger circuit. Resistor R11 and diode CR12 provide a clamped +0.5 V level when S15 is in the + position.

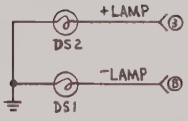
Trigger Input and Selector

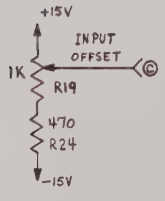
Switch S10 selects either an internal trigger signal derived from the input amplifier, an external input, or the external input divided by 10. Switch S9 selects either a DC, AC Slow or AC Fast signal by integration or differentiation. The wiper of S9 is connected to the input of the trigger amplifier on the linear board.

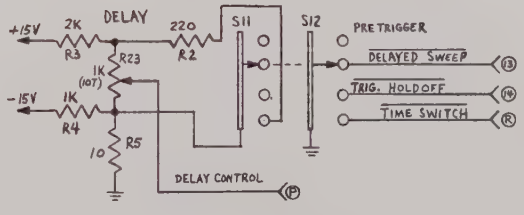

VOLTS FULL SCALE
S1
S2
MV
MVX10
V/10
V
10
20
50
EXT
CR1
CR3
CR2
10X
100X
1X
10X
2K
R1
EXT. V
X1Y
X2Y
+15V

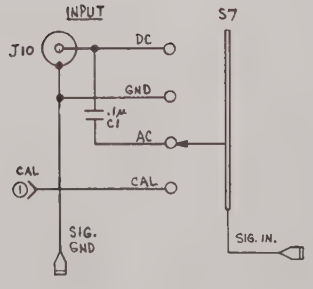

PLOT
S3
PLOT P.B.
⑦

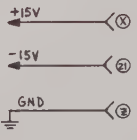

SWEEP TIME A
SWEEP TIME B
+15V
2K
CR4
CR6 CR5 CR7
CR11
CR9
T1
T2
100μSec.
MS
10MS
100MS
Sec.
EXT
S4
S5
S6
S8
CR10
CR8
EXT. T.
5Sec.
500ms
50ms
5ms
500μS
X2T
X1T

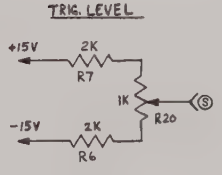

+LAMP
DS2
-LAMP
DS1

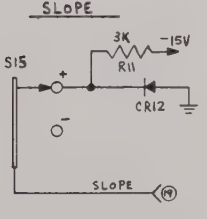

+15V
INPUT
OFFSET
1K
R19
470
R24
-15V

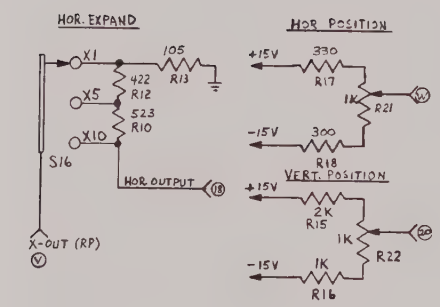

+15V
2K
R3
DELAY
220
R2
S11
S12
PRE TRIGGER
DELAYED SWEEP
TRIG. HOLDOFF
TIME SWITCH
R23
1K
(10T)
-15V
1K
R4
10
R5
DELAY CONTROL

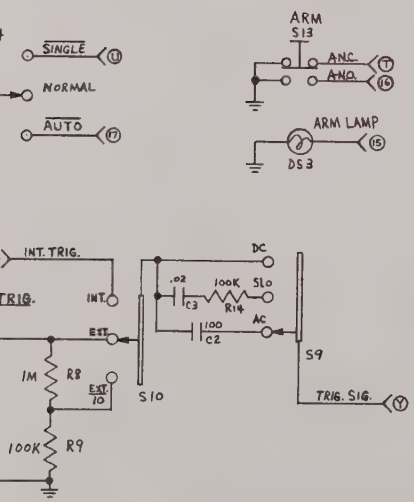

INPUT
S7
J10
DC
GND
.1μ
C1
AC
CAL
CAL
SIG.
GND
SIG. IN.

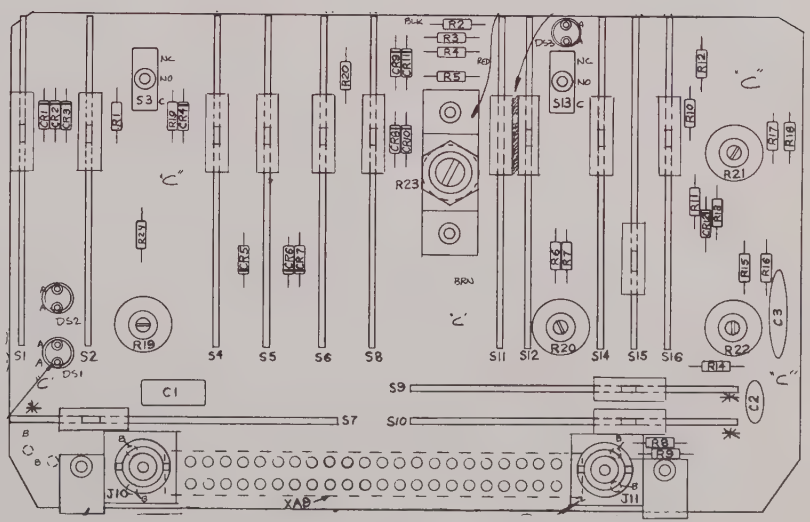

+15V
-15V
GND


TRIG. LEVEL
+15V
2K
R7
1K
R20
-15V
2K
R6


SLOPE
S15
3K
R11
-15V
CR12
SLOPE







FRONT PANEL ASSEMBLY

Schematic & Assembly Drawing

INPUT AMPLIFIER

The input amplifier consists of an input attenuator followed by two cascaded stages of amplification. The two stages are essentially identical except the first stage employs a Field Effect Transistor (FET) input and the second stage utilizes bi-polar transistor inputs. Each stage has switchable gain from a low factor of 4.2 to a high factor of 22, utilizing reed relays in the feedback circuit. The second stage has a fixed gain of 22.

Input Attenuator

The input attenuator is comprised of relays RY1-RY4 and associated resistors and capacitors. In the 10 mV position, RY1 is closed (shorting out the 1 megohm resistor R2). The resultant attenuator factor is 0. In the 100 mV position, RY2 is closed (placing a 124K resistor in parallel with R1). Resistor R2 is then in series with R1, producing an attenuation factor of 10:1. At the 1 V position, RY3 is closed placing a 10K resistance in parallel with R1 (with R2 in series). The attenuation factor is 100:1. At the 10 V position, RY4 is closed placing a 1K resistor in parallel with R1 (with R2 in series). The attenuation factor is 1000:1. Capacitors C15, 17 and 19 are frequency compensation capacitors that are adjusted for flat response with a square wave or pulse input.

Input Stage

Resistor R3 provides for current limiting in the event of voltage overload at the input. Diodes CR1 and CR2 are used to limit the voltage at the gate of Q1 to $\pm$15 V. Potentiometer R7 is used to balance the two sections of Q1. A matched pair of mechanically joined FET's is used in the Q1 position which have their drains tied to the bases of Q2 and Q3. The collector of Q3 is connected to the base of Q4. Capacitor C22 provides an AC feedback path to the gate of Q1 to control the overall response of the stage. Transistors Q4 and Q5 are a unity gain temperature compensated output stage. Diodes CR5 and 6 provide a $\pm$0.5 V clamp on the output. The output of the input stage is connected to the input of the second stage through a series resistor, R25. The output is also fed back through R18 to the inverting input of the amplifier. With the front panel switch in the X5 position, the contacts or relays R5 and R6 are both open and the gain of the stage is 4.22.

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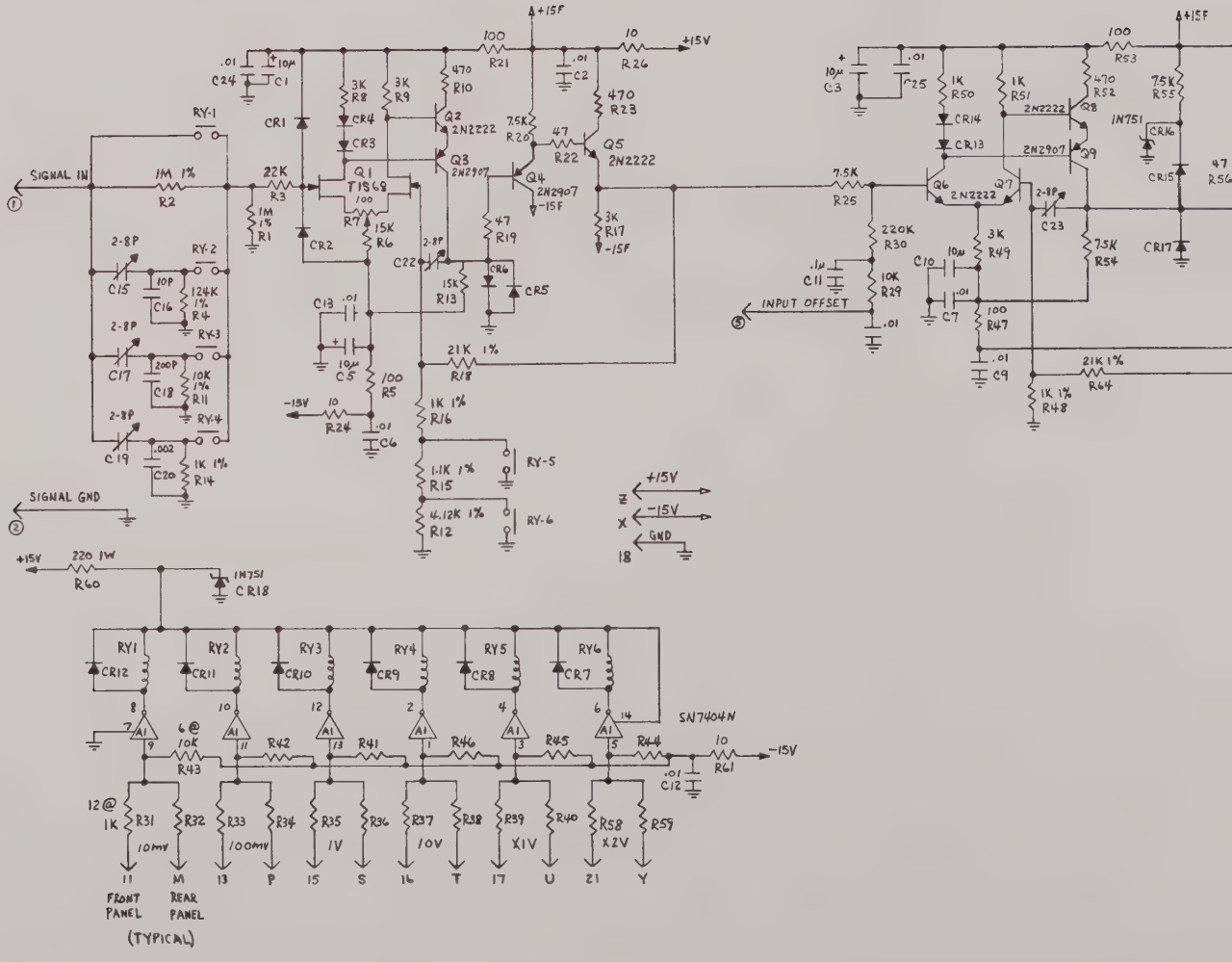
With RY6 closed, the gain is 10.1 and with RY5 closed, the gain is 22. Waveform W1 shows a typical square wave output with a full scale square wave input.

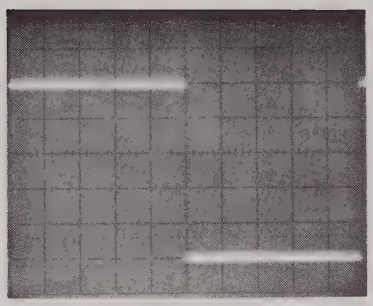
Output Stage

The output amplifier stage is basically the same as the input stage except for the use of bi-polar transistors in the input section. The "input offset" from the front panel provides a DC level to the input of Q6 proportional to the position of the input offset control on the front panel. The overall gain of this stage is 22 and the output range is 0 V to +5 V. Nominal output with a full scale input is 4.8 V p-p. Waveform W2 shows a typical full scale square wave output with a full scale square wave input.

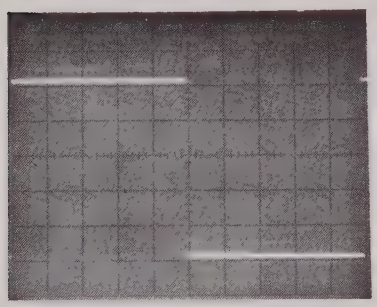
Control

The reed relays used in the control of the amplifier are driven by a hex inverter (SN 7404N) A1. The individual inputs to the inverter are referenced to -15 V through 10K resistors. When a level of at least +4 V is applied to the input control terminals by either the front panel switch or the rear panel connector, the input of the inverter is driven sufficiently positive to close the contacts of the relay connected to that driver. Power for the relays and the SN 7404N is derived from the +15 V supply through a 220 ohm resistor R60 and a 5 V Zener diode CR18. Diodes CR7 through 12 are used to suppress inductive voltage spikes during turn-on/off of the relays.

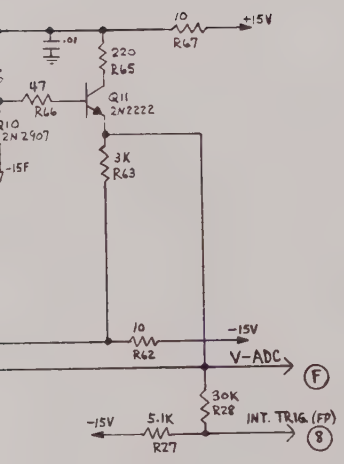

SIGNAL IN
SIGNAL GND
INPUT OFFSET
+15V
-15V
GND
RY-1
RY-2
RY-3
RY-4
RY-5
RY-6
Q1 T1568
Q2 2N2222
Q3 2N2907
Q4 2N2907
Q5 2N2222
Q6 2N2222
Q7 2N2907
Q8 2N2222
Q9 2N2907
SN7404N
FRONT PANEL
REAR PANEL
(TYPICAL)

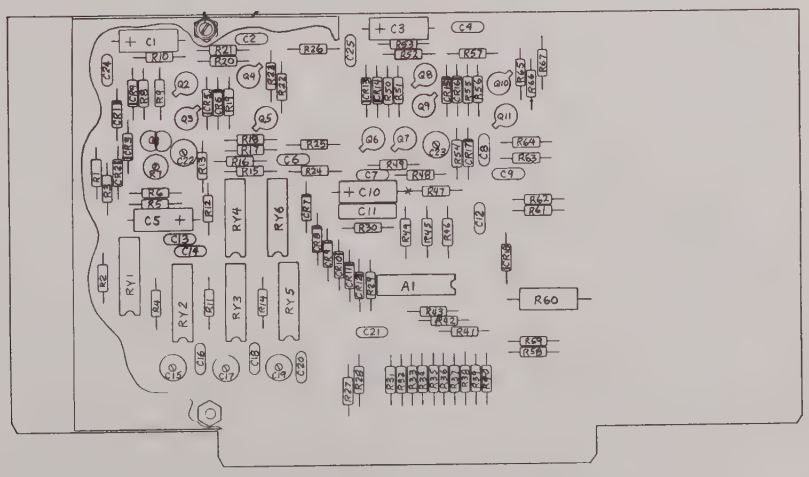


W1 Preamp Output
Loc: Emitter Q5. Scope: V .05 V/Div. Horz. 0.1 ms/div. Trig: Ext. generator sync pulse. Input: 1 kHz square wave 5 V p-p. 802: Volts Full Scale 1 V, X5.



W2 Amplifier Output
Loc: Emitter Q11. Scope: V 1.0 V/div. Horz. 0.1 ms/div. Trig: Ext. generator sync pulse. Input: 1 kHz square wave 5 V p-p. 802: Volts Full Scale 1 V, X5.





INPUT AMPLIFIER

Schematic & Assembly Drawing

ANALOG-TO-DIGITAL CONVERTER

The analog-to-digital converter (ADC) used in the Model 802 is a dual rank converter. This means that the ADC takes two complete conversions of the analog signal to arrive at the final digital equivalent. As a result, the ADC divides down into two sections on two circuit boards. Each section provides 4 bits of the total 8 bits of data. Each section is a parallel discriminator type of converter. The output of the ADC is in Gray Code. The "first rank" converter provides the 4 most significant bits and the "second rank" provides the 4 least significant bits of digital data.

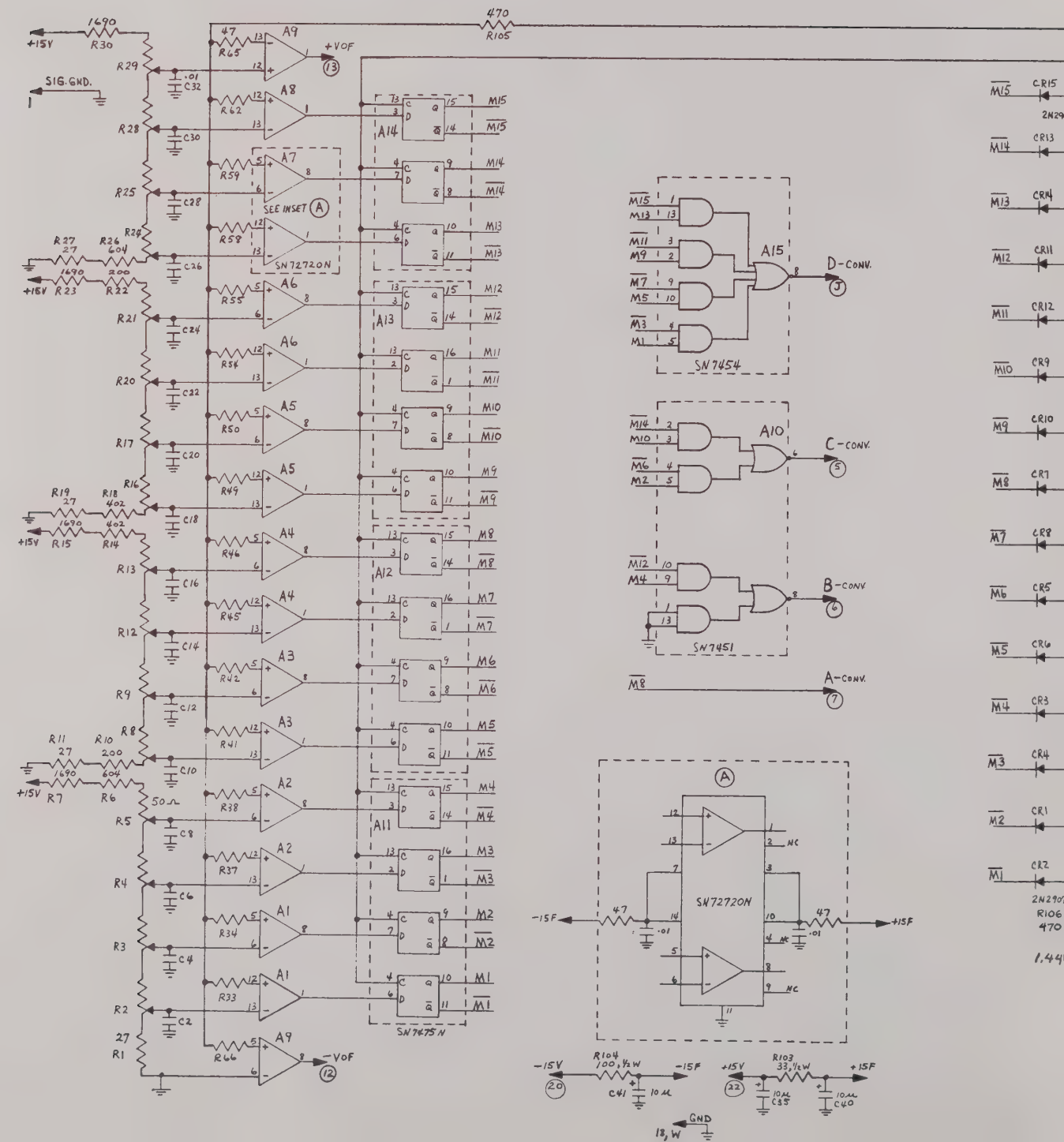
First Rank ADC

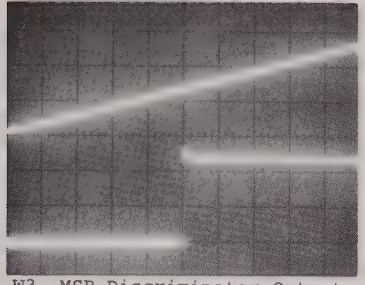
The first rank ADC utilizes 16 parallel differential discriminators, A1-A9. Each discriminator is a high gain amplifier enclosed in pairs in a dual in-line package. The discriminating elements are connected in groups of four and each element has a trim pot to adjust the discrimination level. By breaking the 16 discriminators into groups of four, the cumulative effects of temperature drift and loading are reduced. Each point of discrimination is approximately .300 V from the adjacent points. The adjustment of these points is not extremely critical and is covered in the Calibration Procedure section of this manual.

Waveform W3 shows a typical output from one of the discriminators with a ramp input. The output of the discriminators are connected to a series of quad latches, A11-14. These latches transfer the outputs of the discriminators to the outputs of the latches when clocked by the sample-and-hold pulse from the control logic. A digital value is thus obtained which is accurate to the nearest 1 part in 16. The outputs of the latches are then applied to gates A10 and A15, which convert the digital values to Gray Code. The outputs marked A, B, C and D-CONV comprise the most significant bits of data. It should be noted that two discriminators are required to generate a data bit. One discriminator develops the positive transition and the second the negative transition. If either discriminator fails to generate its transition, improper data will be stored in the memory and the reconstructed output will not be correct. Waveforms W4-W5 show the resultant Gray Code outputs with a ramp input.

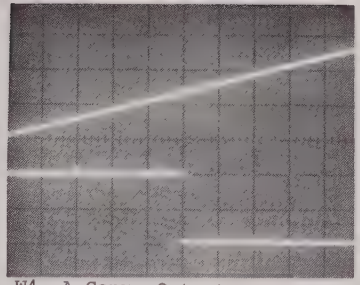
Summation I (ΣI)

The outputs of the quad latches are applied to the emitters of a series of transistors, Q3-Q17. These transistors develop a current proportional to the digital numbers stored in the quad latches. This output is called Summation I (ΣI). The output is used by the second rank converter in developing the least significant bits of data. Transistor Q18 is a reference source whose emitter is at 1.4 V. Waveform W8 shows the sample-and-hold pulse as it comes from the control logic. This pulse is approximately 40 nsec wide and its repetition rate is determined by the sweep time selected.

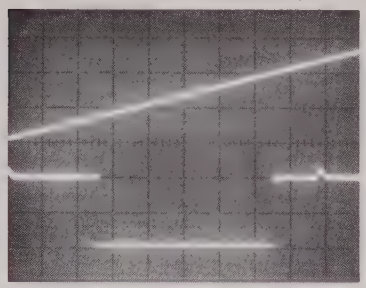

+15V
1690
R30
SIG. GND.
R29
.01
C32
R28
C30
R25
C28
R27
27
R26
604
R24
C26
1690
+15V
R23
200
R22
R21
C24
R20
C22
R17
C20
R19
27
R18
402
R16
C18
1690
+15V
R15
402
R14
R13
C16
R12
C14
R9
C12
R11
27
R10
200
R8
C10
1690
+15V
R7
604
R6
50Ω
R5
C8
R4
C6
R3
C4
R2
C2
27
R1
A9
R65
A8
R62
A7
R59
SEE INSET (A)
R58
SN72720N
A6
R55
A6
R54
A5
R50
A5
R49
A4
R46
A4
R45
A3
R42
A3
R41
A2
R38
A2
R37
A1
R34
A1
R33
A9
R66
+VOF
(13)
-VOF
(12)
470
R105
A14
A13
A12
A11
SN7475N
M15
M14
M13
M12
M11
M10
M9
M8
M7
M6
M5
M4
M3
M2
M1
A15
SN7454
D-CONV.
(J)
A10
C-CONV.
(5)
SN7451
B-CONV.
(6)
A-CONV.
(7)
(A)
SN72720N
NC
47
.01
-15F
+15F
R104
100, ½W
C41
10 M
(20)
R103
33, ½W
C35
C40
10M
(22)
GND
18, W
CR15
2N29
CR13
CR14
CR11
CR12
CR9
CR10
CR7
CR8
CR5
CR6
CR3
CR4
CR1
CR2
2N290
R106
470
1.44



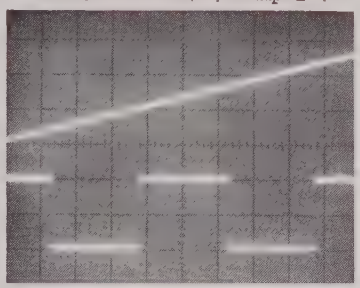
W3 MSB Discriminator Output
Loc: A4 pin 8. Scope: CH 1 1 V/div, CH 2 2 V/div. Horz. 50 µs/div ext. trig. 802: VFS 1 V, X1. Sweep time 500 µs X1. Input: 500 µsec, ramp 1 V



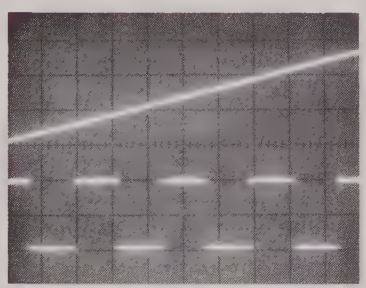
W4 A Conv. Output, MSB.
Loc: Board pin 7. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz. 50 µs/div ext. trig. 802: VFS 1 V, X1. Sweep time 500 µs X1. Input: 500 µs, ramp 1 V



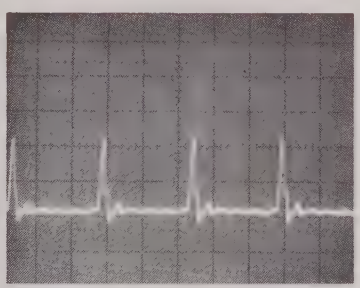
W5 B Conv. Output.
Loc: Board pin 6. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 50 µs/div ext. trig. 802: VFS 1 V, X1. Sweep time 500 µs X1. Input: 500 µs, ramp 1 V



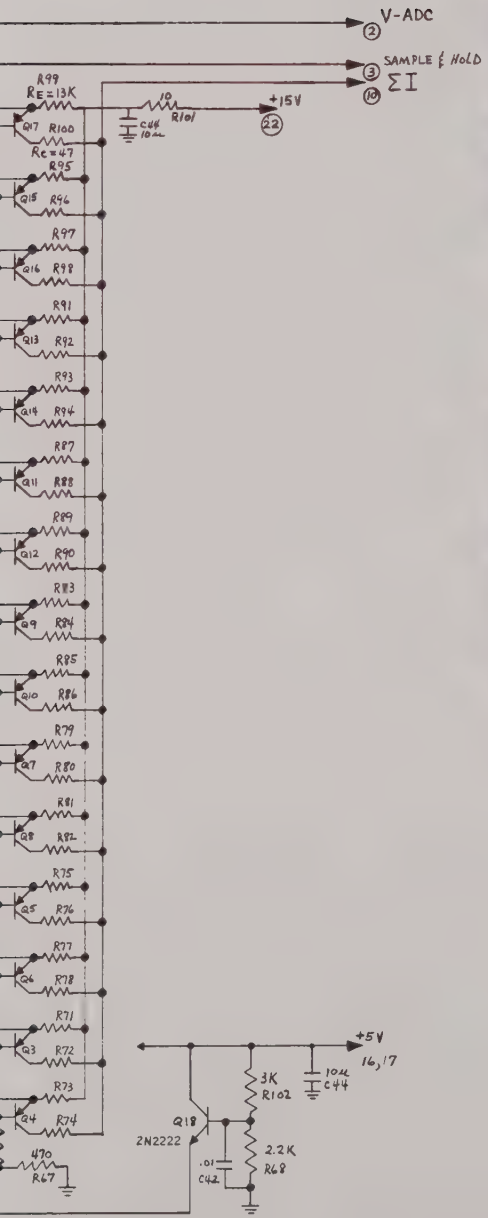
W6 C Conv. Output.
Loc: Board pin 5. Scope: CH 1 2 V/div, CH @ 2 V/div. Horz: 50 µs/div ext. trig. 802: VFS 1 V, X1. Sweep time 500 µs X1. Input: 500 µs, ramp 1 V p-p.

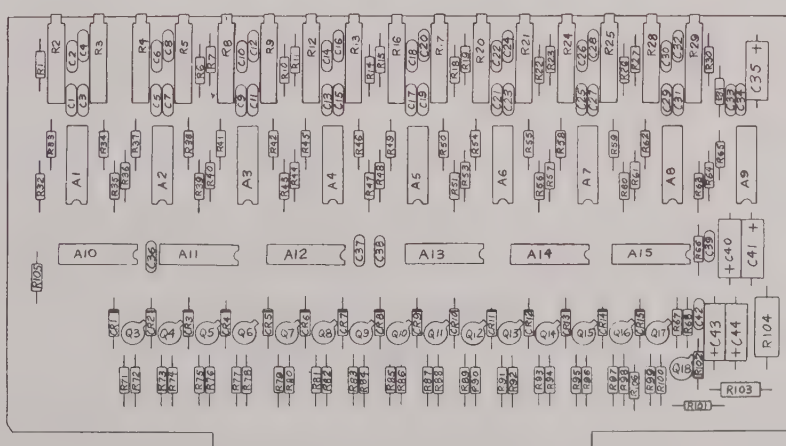


W7 D Conv. Output
Loc: Board pin J. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 50 µs/div ext. trig. 802: VFS 1 V, X1. Sweep time 500 µs X1.



W8 Sample & Hold Pulse
Loc: Board pin 3. Scope: CH 1 1 V/div. Horz: 0.2 µs/div. int. trig. 802: pretrigger record. Sweep time 500 µs X1.





ANALOG-TO-DIGITAL CONVERTER (1st Rank)

Schematic & Assembly Drawing

Second Rank ADC

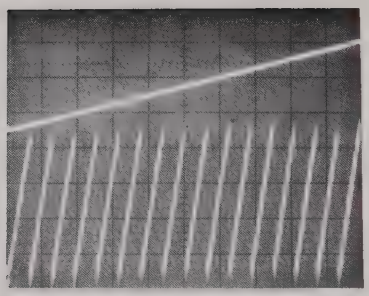
The second rank converter takes the current supplied by the ΣI and subtracts this current from the analog signal. The result is then amplified by a factor of 16 and supplied to the discriminator string. The discriminator produces a four bit output which are the four least significant bits.

Summing Amplifier

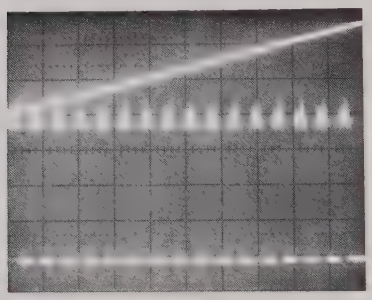
The summing amplifier takes the remainder of the subtraction of Summation I and the output of the input amplifier and amplifies this signal by a factor of 16. Transistor Q3 is a common base amplifier. The base emitter junction is compensated by a diode CR9 to keep the input level constant with changes in temperature. The negative output level is limited by clamp diode CR8 and Zener diode CR10 to about -5 V. The positive level excursion is limited by Q3 to about 0 V. This prevents overvoltage being applied to the discriminator string. The output of this amplifier is buffered by complementary emitter followers Q2 and Q1 to provide temperature compensation and a low impedance to the discriminator. Waveform W9 shows the relationship between the V-ADC input and the output of the summing amplifier. There are three adjustments on the summing amplifier. Potentiometer R114 adjusts the amplitude of the V-ADC signal subtracted from the Summation I and thus controls the output of the summing amplifier. Transistors Q4 and Q5 provide a constant current source as a reference level to the summing amplifier. Potentiometer R102 adjusts the DC level of the output from the summing amplifier. Potentiometer R94 provides a balance adjustment for the summing amplifier. Proper adjustment procedures are given in the Calibration section of this manual.

Discriminator Section

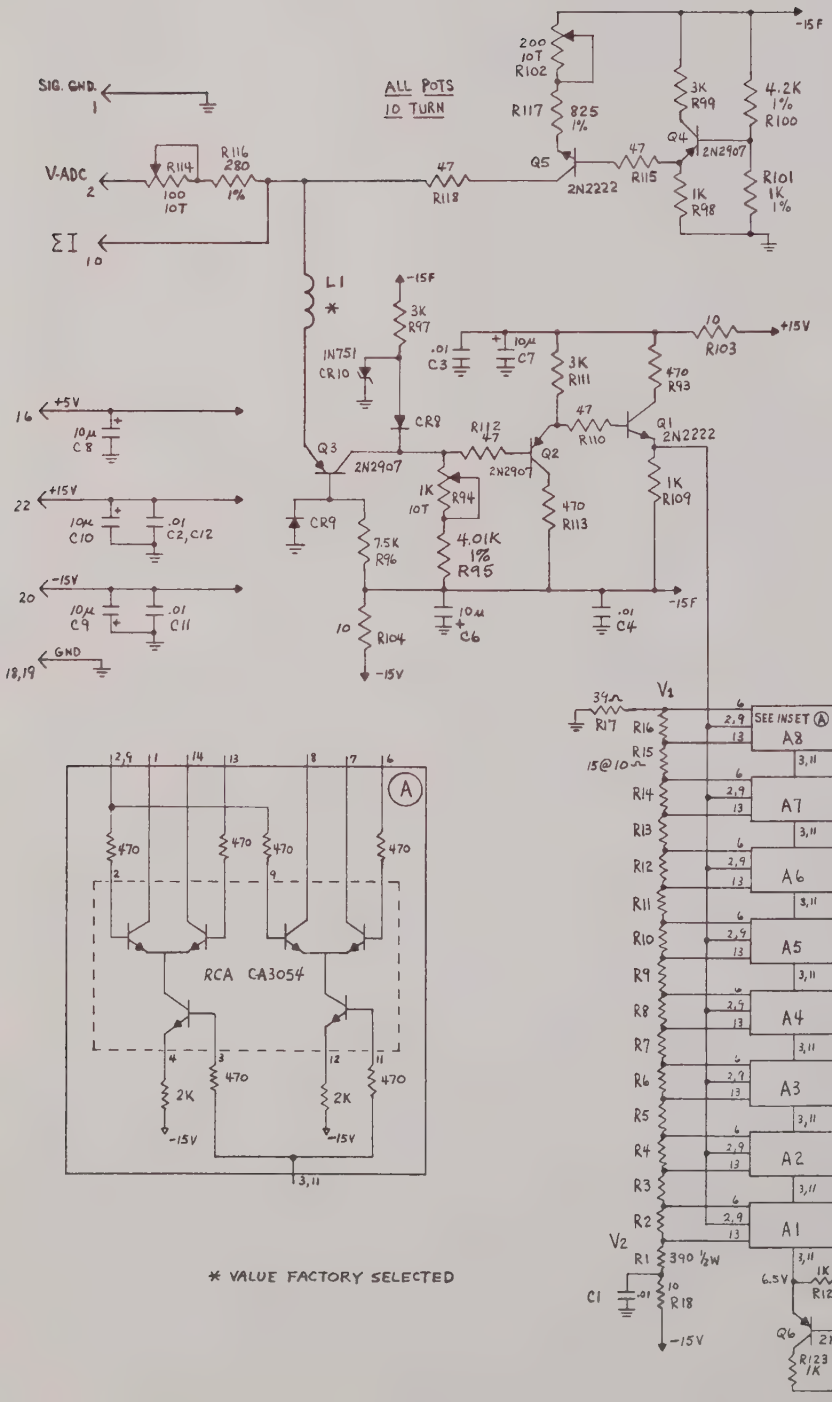
The discriminators used in the second ADC are different from the types used in the first ADC. The discriminators are emitter coupled devices with high bandwidth and open collectors. They are operated in an open loop configuration. The digital information is obtained by summation of the collector currents in a resistor. Again, as in the first rank converter, two discriminators are needed to develop a bit of data, one for positive and one for the negative transition. Waveform W10 shows a typical output from a discriminator. The diode on the output prevents the output of the discriminator from going negative. Transistors Q7-Q10 are emitter follower buffers which drive a quad latch. The strobe pulse to the quad latch transfers the data present at the inputs to the output of the latch. The strobe pulse on the second ADC lags the strobe pulse to the first ADC by 250 nsec. This is to allow for the summation process and settling time for the amplifier. If the signal present at the input changes at a rate faster than 200 nsec, an error can be introduced in the data. However, since the highest sampling rate is 500 nsec, the amount of error is for the most part insignificant. Waveform W11 shows the strobe pulse as generated by the control logic. Waveforms W12-W15 show the outputs of the second rank converter with a ramp input to the ADC.

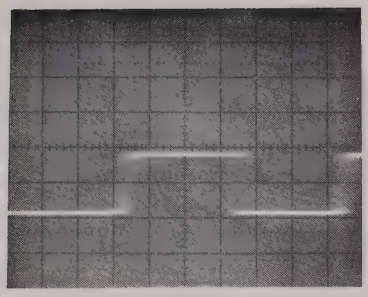


W9 V ADC/V 2nd ADC
Loc: Emitter Q1. Scope: CH 1 2 V/div, CH 2 1 V/div. Horz: 50 µs/div.ext. trig. 802: pre-trigger record. Sweep time 500 µs, ramp 1 V p-p. VFS 1 V, X1.

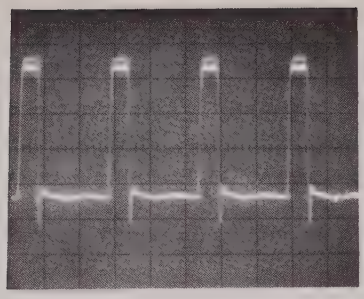


W12 E Conv. Output/Ramp.
Loc: A9 pin 11. Scope: CH 1 1 V/div, CH 2 2 V/div. Horz: 50 µs/div. ext. trig. 802: pretrigger record. Sweep time 500 µs X1.

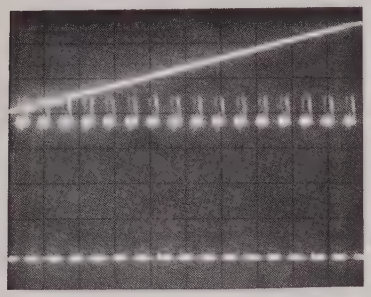




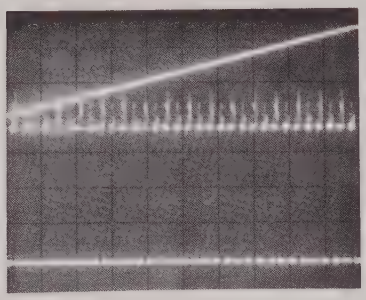
W10 2nd ADC MSB Discrim. Output. Loc: A4 pin 7. Scope: CH 1 1 V/div. Horz: 0.5 µs/div 802: pretrigger record. Sweep time 500 µs X1.



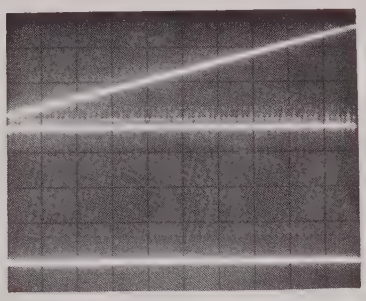
W11 Strobe 2nd Rank Pulse. Loc: A9 pin 4. Scope: CH 1 1V/div. Horz: 0.2 µs/div. int. trig. 802: pretrigger record. Sweep time 500 µs X1.



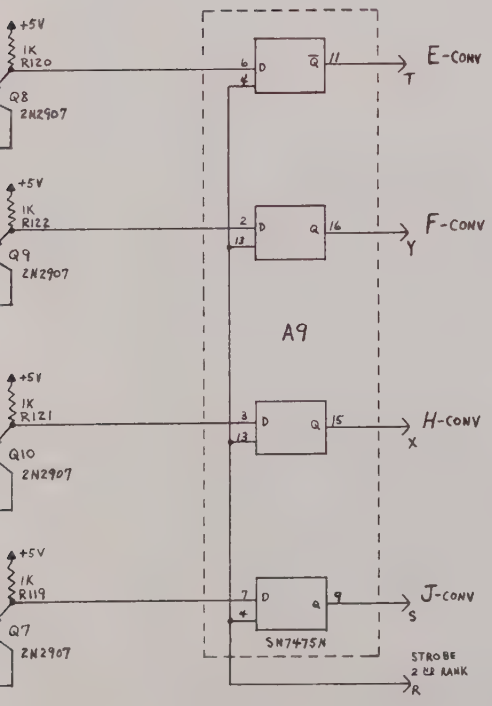
W13 F Conv. Output. Loc: A9 pin 16. Scope: CH 1 1 V/div, CH 2 2 V/div. Horz: 50 µs/div. ext. trig. 802: pretrigger record. Sweep time 500 µs X1.

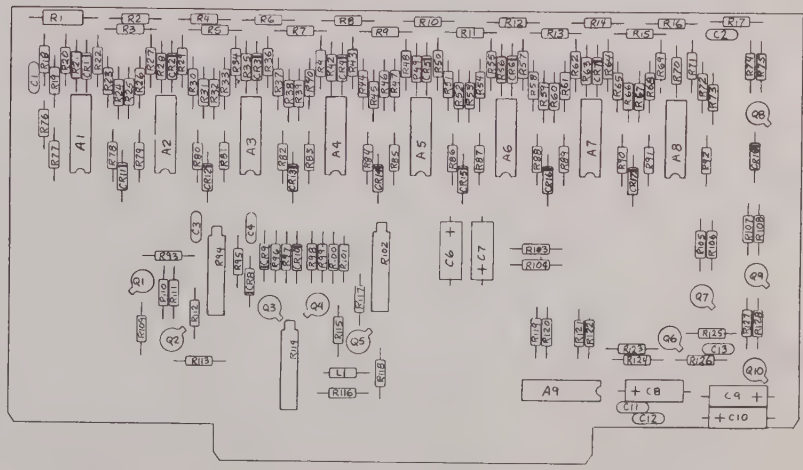


W14 H Conv. Output. Loc: A9 pin 15. Scope: CH 1 1 V/div, CH 2 2 V/div. Horz: 50 µs/div. ext. trig. 802: pretrigger record. Sweep time 500 µs X1.



W15 J Conv. Output. Loc: A9 pin 9. Scope: CH 1 1 V/div, CH 2 2 V/div. Horz: 50 µs/div. ext. trig. 802: pretrigger record. Sweep time 500 µs X1.





ANALOG-TO-DIGITAL CONVERTER (2nd Rank)

Schematic & Assembly Drawing

CONTROL #1 BOARD

The control logic for the Model 802 is divided between two circuit boards labeled Control 1 and Control 2. The logic functions performed by the Control 1 board are: trigger mode selection and generation, operation mode selection, record, output, plot, time base selection and display control.

Trigger & Record Logic (Non-interlace)

The analog signal applied to the Model 802 is discriminated by the trigger circuits on the linear board. The output from the linear board is connected to the Control 1 board at pin D. A typical signal is shown in Waveform W16.

Let's assume that the trigger mode selector is in Normal, that the operating mode selected is Trigger Holdoff, and the sweep speed selected is 5 msec. Under these conditions the instrument is in Display and the trigger flip-flop A15 is reset. The trigger signal produced by the linear board is applied to the clock input of A15. Flip-flop A15 will change state on the positive transition of the trigger signal. The $\overline{Q}$ output is applied to the input of A2 and the Q output is delayed through R6 and C6 (R5 is a pull-down resistor). The $\overline{Q}$ output is also applied to A2. A 0.5 μsec pulse will be produced at the output of A2 (Waveform W16). This pulse is applied to the inputs of A7 pin 12 and A13 pin 12. The pulse will not start a delay cycle because A7 is held off by the $\overline{\text{Holdoff}}$. The trigger pulse will appear in the output of A13 pin 11 since we are in the Holdoff mode. This pulse will also pass through A23 because we are not in interlace (interlace is true at sweep speeds of 2 sec or greater). The output of A23 pin 4 is inverted by A23 and applied to the input of A10 which is connected as a flip-flop causing Record to go true (Waveform W17). When the Record flip-flop A10 changes state, a pulse is generated at A16 pin 11 (Waveform W18). The $\overline{\text{Record Reset}}$ pulse is applied to A4 to reset the two memory counters AC and M (Waveform W19). The $\overline{\text{Record Reset}}$ pulse is applied also to the input of A4 pin 1 which is used as an "Or" gate, thus causing the time base to be reset. During Record, data is stored in the memory at the rate set by the sweep time control. Counters AC and M located on the time base and address board count up to 1024. At the negative transition of last counter of the M register ($X2^9$), a pulse is generated by gate A11 (Waveform W20). This pulse goes through gate A23 and A16 and resets the Record flip-flop (A10), thus ending the Record cycle. The unit then returns to the Display mode for a period of time determined by the control logic as follows. The AC memory counter overflows at the same time as the M counter and generates a Z pulse. This pulse is shaped by gate A11. At the end of Record, the Z pulse is inhibited at A23 by the delay circuit (R27-C19). At the completion of one display sweep, Z again produces a pulse which is passed by gate A23 and gate A7 to initiate the delay cycle.

Waveform W21 shows the relationship of these signals. If the delay control is set to minimum, and end of delay ($\overline{EOD}$) pulse occurs within 200 nsec and is gated by A8, resetting the trigger flip-flop A15, rearming the trigger circuit.

Trigger & Record Logic (Interlace)

As mentioned previously, at sweep speeds of 2 sec or slower, the data is interlaced into the memory. During interlace the memory is clocked at a high speed rate and the data is placed into the memory one compartment later on each circulation. In interlace the operation of the trigger flip-flop A15 will be the same as described before. The pulse generated at A2 pin 1 will pass through A13; however, it will not go through A23, instead it will reset flip-flop A21. At the next AC overflow, which will occur within 2 msec (in Display the memory is clocked at 2 μsec), flip-flop A21 will be set and the AC overflow will pass through gate A17 setting the Record flip-flop. Waveform W22 shows the relationship of these signals during the start of a record cycle. The record cycle will end when the M counter ($X2^9$) overflows and the resultant pulse at A11 pin 8 resets the Record flip-flop.

Delayed Sweep Operating Mode

In the Delayed Sweep mode, the record cycle begins only after the completion of the delay cycle. In Delayed Sweep, the pulse generated at A2 pin 1 is gated through A7 and initiates a delay cycle. After completion of the delay cycle, the end of delay ($\overline{EOD}$) will indicate that the delay cycle has ended. The $\overline{EOD}$ pulse is gated by A13 and will set the Record flip-flop as described in the Trigger Holdoff mode.

Switched Time Base Mode of Operation

In the Switched Time Base mode, the trigger pulse from A2 pin 1 is gated through to the Record flip-flop in the same manner as in Trigger Holdoff. However, the delay cycle is also initiated. The Record output allows flip-flop A3 to be set after the end of delay by the negative transition of Delay through gate A2. If the delay is set at minimum, flip-flop A3 will be set within 200 nsec of the trigger pulse so all of the data will be recorded at the rate set by Sweep Time B (T2 high, T1 low). As more delay is introduced, more time will be recorded at the A sweep time rate and less at B sweep time rate. Waveform W23 shows the relationship of these three signals. When the outputs of A3 change state, a pulse is generated by gate A10 which in turn resets the time base. The end of cycle ($\overline{EOC}$) input provides clocking pulses to flip-flop A3. Flip-flop A3 is reset by the negative transition of Record and a new cycle can begin.

Pretrigger Record Mode

In the Pretrigger Record mode of operation, Record is initiated by pressing the Arm pushbutton in the Single sweep trigger mode. In this mode a trigger is used to terminate the record cycle. When a trigger occurs, delay is initiated as in the Delayed Sweep mode. The $\overline{EOD}$ signal is gated through A19. The output of A19 pin 8 is gated through A20 and at the end of delay the record flip-flop will be reset, thus ending the record cycle. At sweep speeds of 2 sec or slower (interlace), flip-flop A21 is reset by the $\overline{EOD}$ pulse. At the next EOC pulse, flip-flop A21 is set again, causing the recording to stop. This is done by gating EOC through A19 pin 12, A19 pin 8 and A20 pin 6 to reset the record flip-flop A10. This temporary storage of EOD by A21 is necessary because recording must be terminated when both memory counters agree. EOC is produced only under this condition.

Trigger Modes

There are three triggering modes available in the Model 802: Single, Normal and Auto. In the Single mode, flip-flop A15 can either be reset by pressing the Arm pushbutton or by introducing a remote digital arm signal from the rear panel connector. In the Normal mode, A15 is reset automatically after each record and display cycle. In the Auto mode, a 0.1 sec pulse rate is applied to the "direct set" input of A15. Thus in the absence of a trigger signal A15 will be set every 0.1 sec. The Auto mode is used almost exclusively for setup purposes.

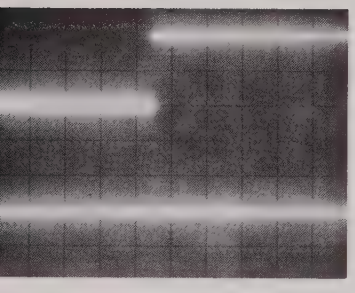
Plot Output Mode

The Plot flip-flop A6 (lower portion) is normally reset and the Plot mode can only be entered when the trigger mode switch is in Single. When the Plot pushbutton is pressed and when the memory is at address 0 (gate A11), flip-flop A6 will be set initiating the Plot Output mode. During Plot the data is strobed out of the memory at the rate of a word every 0.1 sec. At the beginning of Plot, the display is disabled and a Mode pulse is generated by A18. This pulse resets the time base through A4 and places the first data word in the output buffer. The Mode pulse also enables the "plot output" on the linear board. During Plot, the M counter is counting up at the rate of 0.1 sec. When the M counter overflows, signified by the $X2^9$, a pulse is generated by A11 causing another clock pulse at A6 and causing flip-flop A6 to return to its reset state, thus ending the Plot mode.

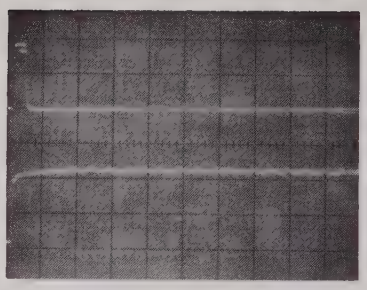
Output Mode

The Output mode is different from the Plot mode in that data is taken out of the memory at an external rate. As in Plot, the trigger selector must be in the Single position. The output cycle is initiated by grounding pin 7 of the rear panel

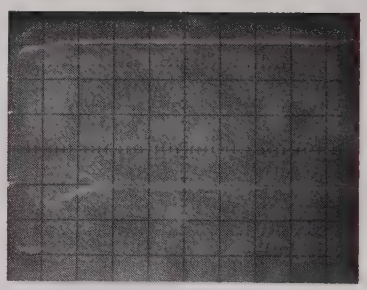
connector J9, which causes the input of A6 (upper portion) to be positive. At the next address 0 flip-flop A6 will be set. The output line must be held at ground for the duration of the output cycle. If the output line is raised to +5 V, the output of data will stop (gate A12). At the beginning of output, a $\overline{\text{Mode}}$ pulse is generated and the time base is reset; also, the display is disabled by the $\overline{\text{P+0}}$ signal. After all 1024 words have been output, the M counter rolls over, causing A6 to be reset. The instrument will return to the display mode. If the output control line is still held at ground, the unit will return to the output mode at the next memory address which occurs 2 msec later.



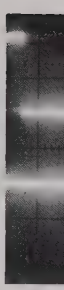
W16 Trigger/Trigger Pulse. Loc: A15 pin 3/A2 pin 1. Scope CH 1 2 V/div, CH 2 2 V/div. Horz: 50 µs/div. int. trig. CH 1. 802: trig. hold-off mode 500 µs X1. Triangle wave input. Normal trigger.



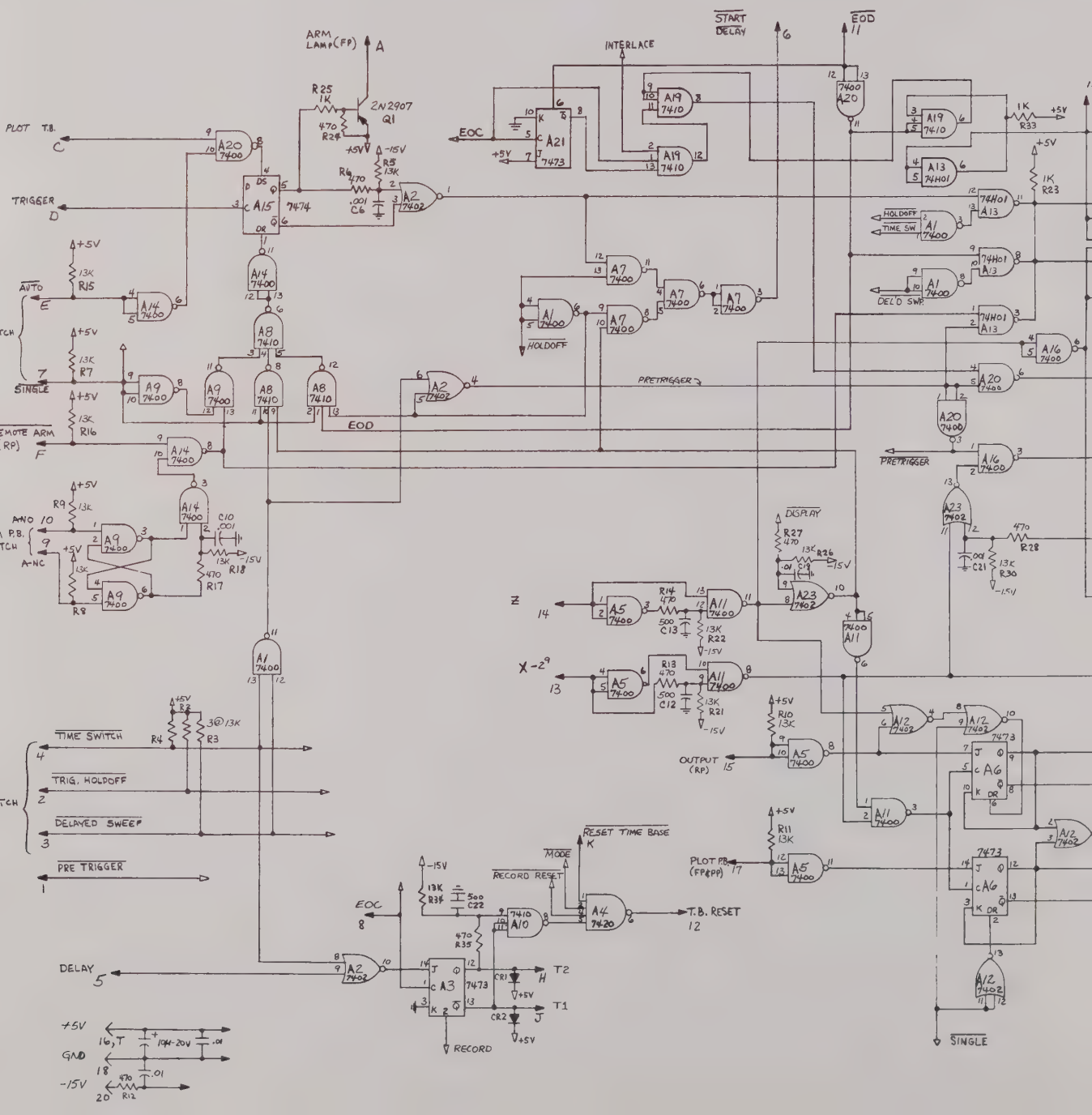
W17 Trigger Pulse/Record. Loc: A2 pin 1/A10 pin 6. Scope CH 1 2 V/div, CH 2 2 V/div. Horz: 1 µs/div. int. trig. CH 1. 802: trig. hold-off mode. Sweep time 500 µs X1. Triangle wave input. Normal trigger.

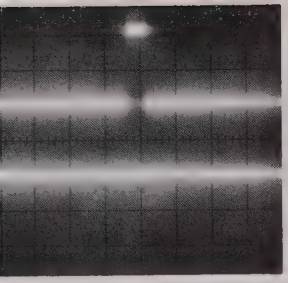


W18 Record/Record Reset. Loc: A10 pin 6/A16 pin 11. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 0.5 µs/div. int. trig. CH 1. 802: trig. hold-off mode. Sweep time 500 µs X1. Trig. in Normal mode.

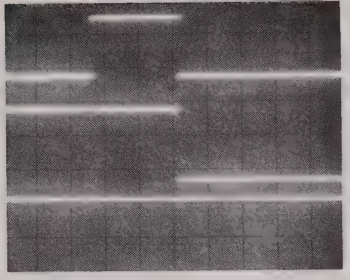


W19
Loc:
CH 1
Horz:
802:
time

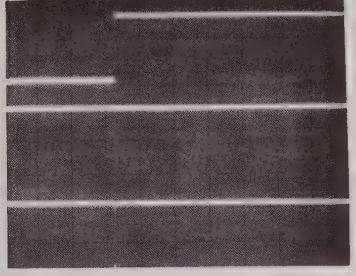




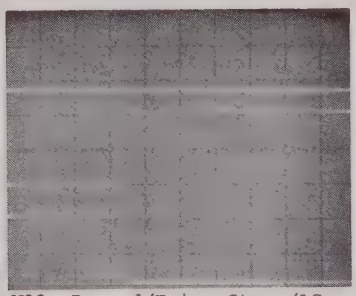
Record/Reset AC & M.
A10 pin 6/A4 pin 8. Scope:
2 V/div, CH 2 2 V/div.
0.1 ms/div. trig. CH 1.
trig. hold-off mode. Sweep
500 µs X1. Normal trigger.



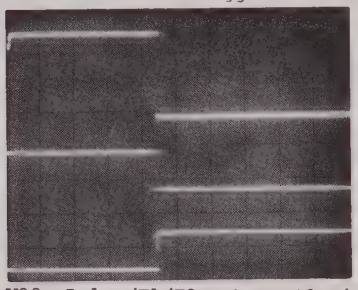
W20 X2[9]/Record/Overflow Pulse
Loc: A5 pin 5/A10 pin 6/A11
pin 8. Scope: CH 1 2 V/div,
CH 2 2V/div, CH 3 2 V/div.
Horz: 0.1 ms/div. trig. CH 2
(record). 802: trig. hold-off.
Sweep time 500 µs X1. Normal.



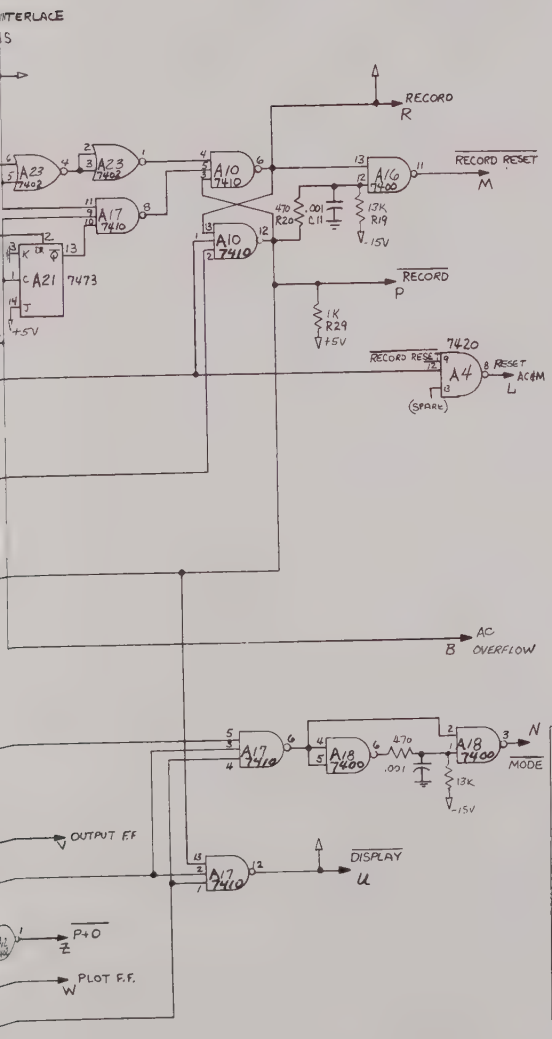
W21 Z/Z Pulse/Rearm.
Loc: A5 pin 1/A11 pin 11/A23
pin 10. Scope: CH 1-CH 3 2 V/
div. Horz: 10 s/div. trig.
CH 1 (Z). 802: trig. hold-off.
Sweep time 500 µs X4. Normal.

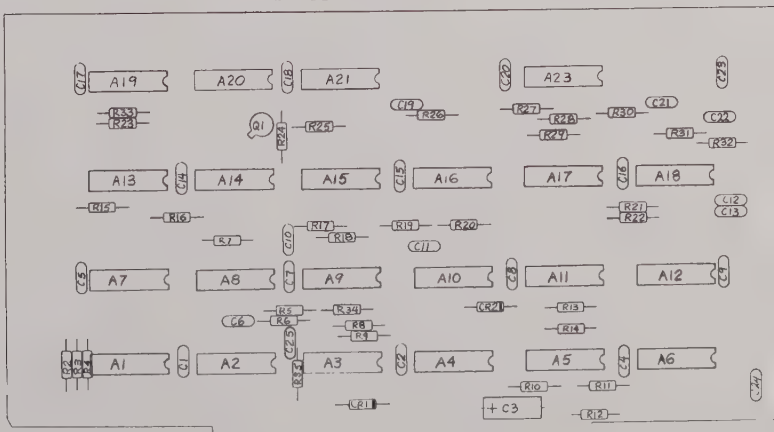


W22 Record/Trig. Store/AC
Overflow. Loc: A10 pin 6/ A21
pin 13/A21 pin 1. Scope: CH 1-
CH 3 2 V/div. Horz: 0.5 ms/div.
trig. CH 2 trig. store. 802:
trig. hold-off. Sweep time 500
ms X4. Normal trigger.



W23 Delay/T1/T2. Loc: A2 pin
9/A3 pin 13/A3 pin 12. Scope:
CH 1 2 V/div, CH 2 5 V/div,
CH 3 5 V/div. Horz: 20 µs/div.
int. trig. on delay. 802:
switched time base. Sweep time
A 500 µs X1, B 500 µs X4. De-
lay approx. 1.40.





CONTROL #1

Schematic & Assembly Drawing

CONTROL #2 BOARD

The logic on the Control 2 board performs the following functions: provides the memory clock pulses at the proper rates; generates the strobe pulses for the analog-to-digital converter and output buffer; generates the AC and M counter advance pulses; controls the output of data during all output modes and generates the flag signals; drives the offscale lamps; and provides the input/circulate logic for the memory.

Memory Clock Control & Generation

The memory clock produces a constant series of pulses at the proper rate and phase to circulate the data in the memory. Gates A19, A15 and A9 are used to control the rate at which the memory will be clocked. During times when the instrument is in the Plot or Display modes, the display time base is gated through gate A9 which is used as an "Or" gate. During Record gate A15 is enabled and the memory is clocked at the rate (time base) selected by the front panel sweep time controls. During those times when the unit is in the Output mode, the memory is clocked by either an external rate of 2 μsec to 500 μsec, or by the display time base as determined by the flip-flop comprised of A3 and A9. The output of A9 pin 6 is called "start cycle". These pulses are gated through flip-flop A16 by the "clock" pulses from the time base generator. At the beginning of each record cycle, the clock generator and phasing flip-flops A16, A17 and A18 are reset by the Record Reset pulse. This is to insure that each record cycle begins in exactly the right phase. The $\overline{Q}$ output of A16 pin 8 is used to generate the AC advance pulse. Thus the AC counter is always synchronized with the memory clock. Waveform W24 shows the clock rate as it changes from Record to Display. Waveform W25 shows the phase relationship between the two clocks and the start cycle signal during Display. The start cycle signal is also used to generate the sample-and-hold signal and the strobe second rank pulse to the analog-to-digital converter.

M Advance

During the record cycle when data is being stored in the memory, the M counter is also being advanced by the M advance logic A12. During record cycles under internal control and at sweep speeds faster than 2 seconds, $\overline{\text{Interlace}}$ A12 pin 1 is enabled by A21 and A22 and the M counter is advanced at the same rate as the AC counter (Waveform W27). When data is being interlaced into the memory (sweep speeds of 2 seconds or slower), A12 pin 10 is enabled by gate A20 and the M counter is advanced one count for each full circulation of the AC counter by the AC overflow pulse from the "time base and address board" (Waveform W28). During the plot cycle, the M advance is generated through A12 pin 11 by the plot time base. During Output the M advance is used to count the word requests and to interlace the data out of the memory at the proper address.

Sample-and-Hold & Strobe 2nd Rank Pulse Generation

The sample-and-hold pulse is generated by each positive transition of the start cycle pulse train by gate A11 and A20. After the propagation and clocking delays of A16 and A17, the strobe second rank pulse is generated by A17 Q. This pulse is gated and inverted by A4. The strobe second rank pulse lags the sample-and-hold pulse by 250 nsec. Waveform W29 shows the relationship between the sample-and-hold pulse and the strobe second rank pulse.

CRT Control

The CRT control logic consisting of gates A1 and A7 is used to gate the "Z" signal to the horizontal ramp generator. The "Z" pulse is 32 µsec wide and occurs every 2 msec (Waveform W30). During the non-interlace record and when the instrument is in the Plot or Output modes, the CRT output is at ground and disables the ramp generator. The CRT signal is also used as a synchronization pulse for the beginning and ending of the ramp.

Flag & Output Strobe

The output strobe pulse is used to clock the data from the memory into the output buffer located on the memory board during Display and Output modes. In Display, the strobe pulse is derived from A17 pin 9 gated by A7 and A13 and occurs at a 2 µsec rate. In the Plot or Output modes, the output strobe pulse occurs immediately upon initiation of these modes by the $\overline{\text{Mode}}$ pulse from Control 1. Subsequent pulses occur when the M counter equals the AC counter (AC = M), gated by A13. Waveform W31 shows the relationship between the output strobe pulse and the start cycle pulse in Display. The flag pulse is used by an external device as a data ready signal. The flag output is normally low when the 802 is placed in the output mode. Flip-flop A14 is set by the trailing edge of the output strobe pulse and the flag line goes high. Flip-flop A14 remains set until the next word command at which time it is reset until the next strobe pulse occurs. Waveform W32 shows the relationship between the output strobe and word command.

External Time Base Control & Word Command Logic

The series of gates located at the left edge of the schematic provide this function. Gates A3 and A9 comprise a flip-flop which is used to prevent the memories from being clocked too slowly during either record with external time bases or during output. Immediately after the start of Record or Output, this flip-flop is set by the $\overline{\text{Record}}$ $\overline{\text{Reset}}$ or $\overline{\text{Mode}}$ pulse so that A9 pin 8 is high.

The pulse generated by the external source (and shaped at A20 pin 13) is gated through A15 and A9. This pulse is used to generate a start cycle and also reset the time base. If the

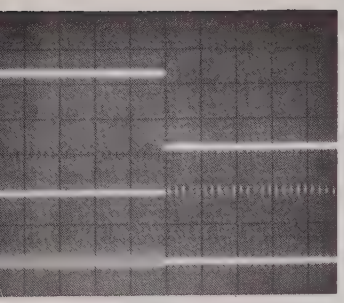
pulses continue at a rate faster than the 500 μsec, the time base will not count up to produce a transition at the 1 msec T.B. input at gate A3. If the time lag between the external pulses exceeds 500 μsec, flip-flo A3, A9 will be reset by the 1 msec T.B. and the display time base will be gated through A15. The external pulse will be inhibited at A15 and will no longer control the memory clocking. Then flip-flop A10 is used to temporarily store the external pulse until a synchronizing clock pulse can occur. Then the sample-and-hold, strobe second rank and M advance pulses are generated. Waveform W33 shows the relationship between the external time base and the pulse at A20 pin 13.

Input/Circulate Logic

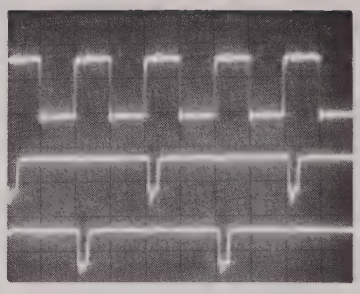
Gate A2 comprises the logic which determines whether data will be input or circulated in the memory. In any mode other than Record, the circulate is high and the input is low. During Record the reverse is true as long as AC equals M. In interlace, AC equals M only once during every full memory circulation. Thus, in interlace-record, the memory is held in circulate until AC equals M. At this time new data is inserted into the memory (Waveform W34). In Record-Interlace AC is always equal to M so that Record must be high and is the controlling signal.

+ and - Lamp Drivers

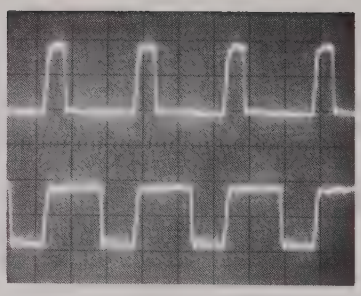
Gate A6 and transistors Q1 and Q2 comprise a set of flip-flops and lamp drivers for the positive and negative offscale lamps on the front panel. If any portion of the input signal exceeds the dynamic range of the analog-to-digital converter, either positive, negative, or both flip-flops will be set and the lamps will be turned on. The AC overflow pulse (inverted by A5) is used to reset the flip-flops.



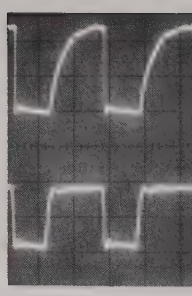
W24 Record/Memory Clock. Loc: A15 pin 13/A23 pin 8. Scope: CH 1 2 V/div, CH 2 2V/ div. Horz: 0.1 ms X10 exp. Trig. on Record. 802: trig. hold-off. Sweep time 500 µs X1. Normal trigger.



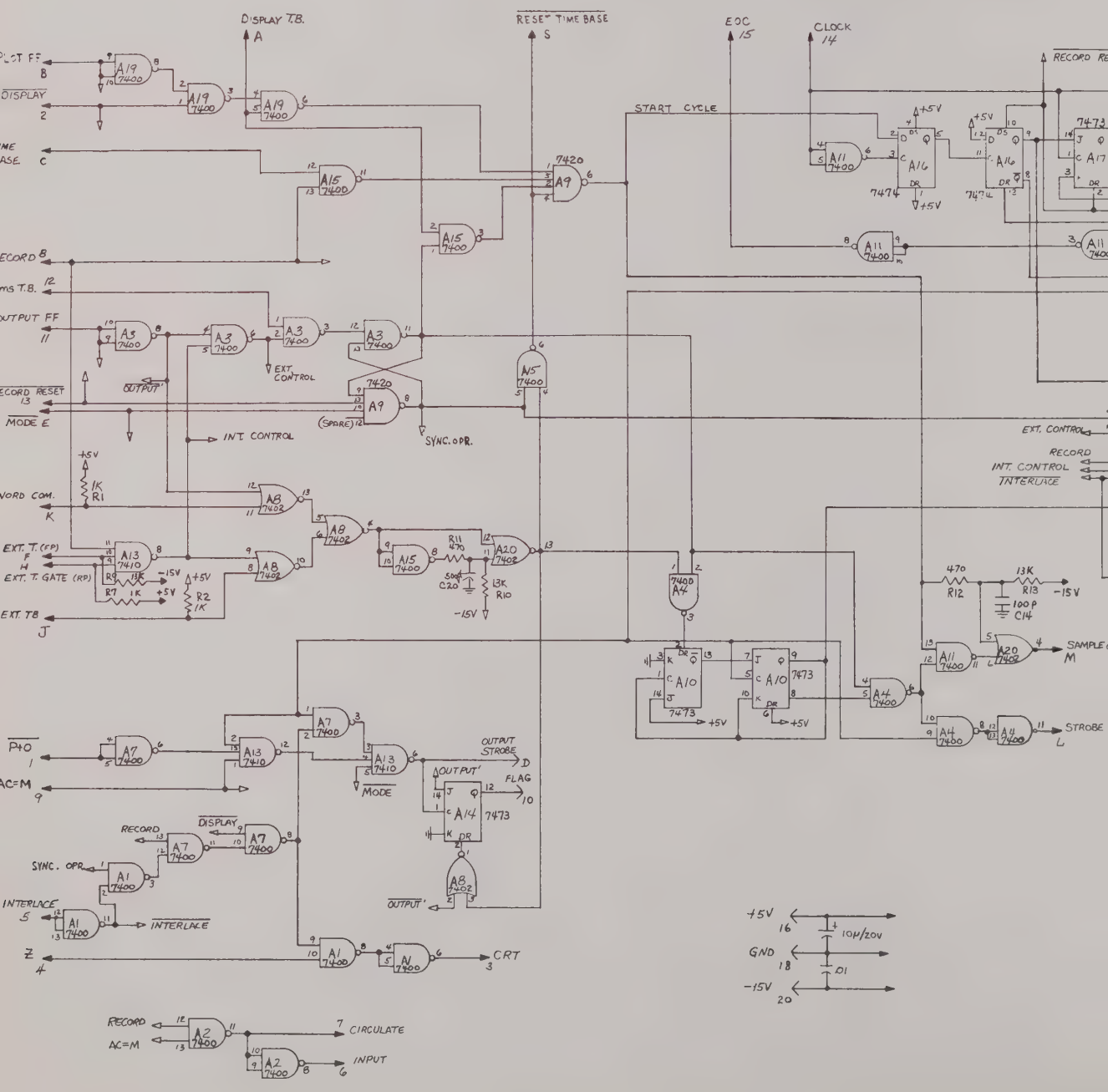
W25 Start/Clock 1/Clock 2. Loc: A9 pin 6/A23 pin 11/A23 pin 3. Scope: CH 1-CH 3 2 V/ div. Horz: 1 µs/div. trig. on start. 802: trig. hold-off. Sweep time 500 µs X1. Single sweep mode.



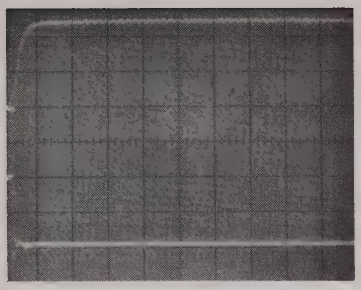
W26 EOC/AD Advance. Loc: A11 pin 8/A23 pin 9. Scope: CH 1 2 V/div, CH 2 2 V/ div. AC Adv. Horz: 0.2 µs/div. trig. on. 802: pretrigger record. Sweep time 500 µs X1.



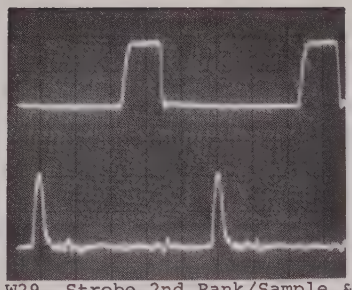
W27 M Advance/ Loc: A12 pin 6/ Scope: CH 1 2 V div. Horz: 0.2 pretrigger reco 500 µs X1.



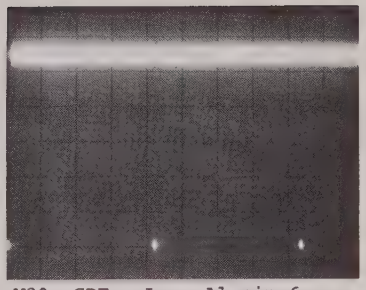
dvance.
pin 9.
, CH 2 2V/
iv. 802:
Sweep time



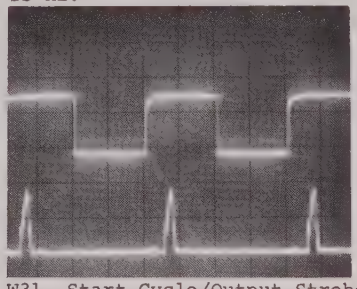
W28 M Advance/AC Overflow. Loc: A12 pin 6/A12 pin 9. Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 0.5 µs/div. trig. on AC overflow. 802: pretrig. record. Sweep time 500 ms X4.



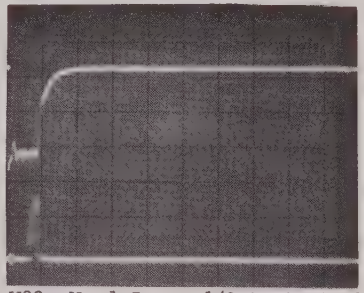
W29 Strobe 2nd Rank/Sample & Hold. Loc: A4 pin 11/A20 pin 4. Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 0.1 µs/div. trig. on sample & hold. 802: pre-trigger record. Sweep time 500 µs X1.



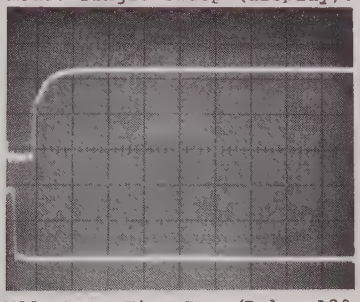
W30 CRT. Loc: A1 pin 6. Scope: CH 1 1 V/div. Horz: 0.5 ms/div. ext. trig. 802: trig. hold-off mode. Single sweep.



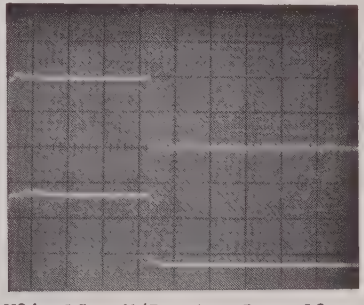
W31 Start Cycle/Output Strobe. Loc: A9 pin 6/A13 pin 6. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 0.5 µs/div. trig. on start. 802: trig. hold-off mode. Single sweep (display).



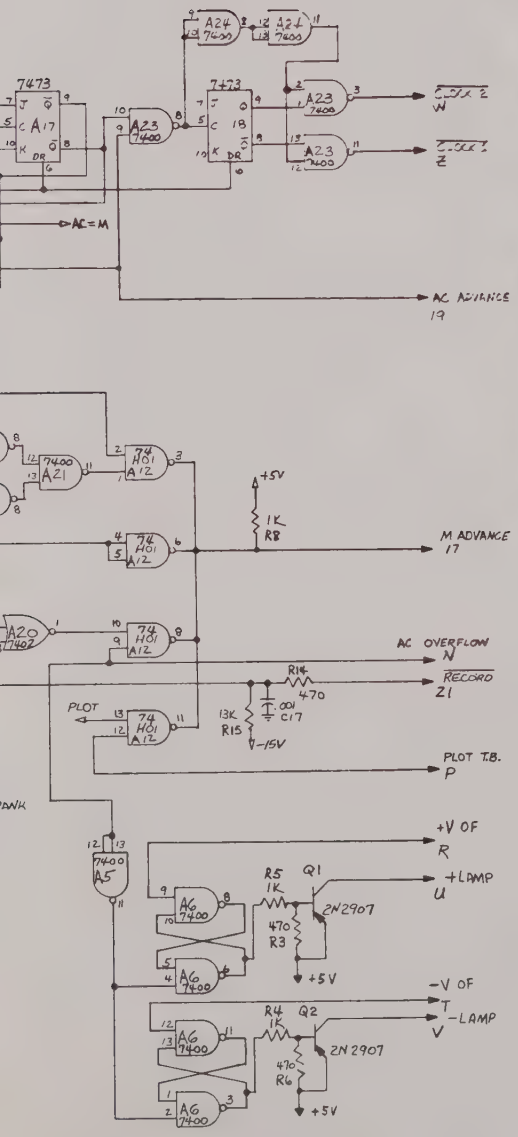
W32 Word Command/Output Strobe Loc: A8 pin 11. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 0.5 µs/div. 802: output mode. Ext. 0.5 µs pulse to word command.

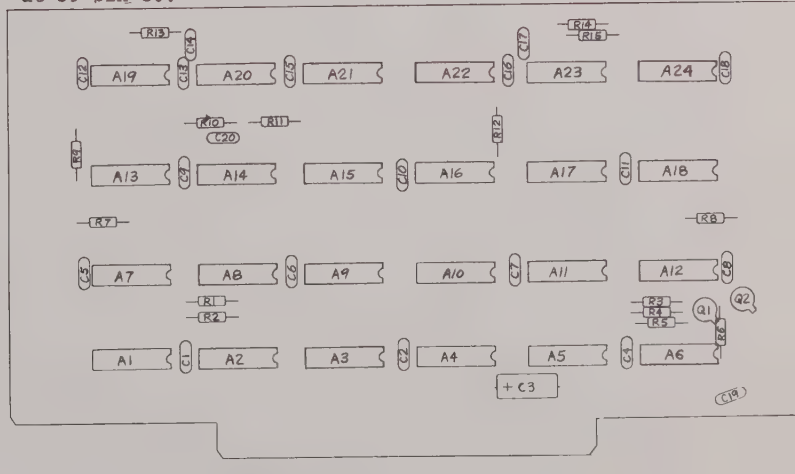


W33 Ext. Time Base/Pulse A20 Pin 13. Loc: A8 pin 13. Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 0.5 µs/div. 802: pretrig. record. Sweep time Ext. 0.5 µs pulse 2 µs rep rate at J9 pin 30.



W34 AC = M/Input. Loc: A2 pin 13/A2 pin 8. Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 0.5 mµs/div. 802: pretrigger record. Sweep time 500 ms X4.





CONTROL #2

Schematic & Assembly Drawing

Memory Board

The digital outputs from the analog-to-digital converter are connected to the inputs of the memory board. The digital data is stored in a 1024 word semiconductor shift register memory during the record cycle. During display the data is recirculated in the memory.

Input Logic

Gates A1, 2, 3, 22 and 23 are used to either input new data or recirculate data already in the memory. When the "input" line is positive, new data is stored. When "circulate" is positive, the data will be recirculated in the memory. The 3K resistors on the outputs of the gates are used to pull the outputs to +5 V.

Clock Driver

Since the memory elements are MOS (metal-oxide-semiconductor) and the storage is a dynamic shift register, the data must be clocked through the memory at all times. The clock driver shapes and amplifies the clock pulses generated by Control #2 board. There are two identical drivers, one for each phase of the clock. Waveform W35 shows the phase relationship between the two clock driver outputs.

Memories

Data is stored in the memories on the trailing edge of the clock pulse. Each clock pulse will move the data one position in the shift register. Since the clock pulses are out of phase, even numbered words will be clocked by one phase and odd numbered words by the second phase. If the number of words placed into the memory exceeds 1024, as occurs in the pretrigger record mode of operation, the last word (1025) will be lost. Thus, the contents of the memory will always be 1024 words. At the end of the record cycle, the repetition rate of the clock pulses changes to the 2 µsec/word rate and the circulate line goes true. The data then recirculates through the inverter, input gate, and the memory.

Output Buffer

Flip-flops A10, 12 and 16 provide an output buffer storage unit. In the display mode, this buffer is clocked by the "output strobe" pulse at a 2 µsec rate. Each word in the buffer is thus held for approximately 2 µsec. During times when data is being taken at slower rates, such as plot or output rates slower than 2 msec, the data is clocked into the buffer and held for longer periods of time. However, the memory continues to circulate at the 2 µsec/word rate. The control logic and the memory tracking counters insure that

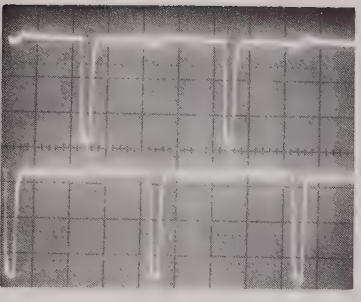
each word placed in the output buffer is the next sequential word. At output rates of 2 µsec to 500 µsec, the memory is clocked at the same rate as the "Word Command" pulse. However, if the control logic senses a time lag between data requests which is greater than 500 µsec, it automatically speeds up the memory to insure that no data is lost. All further requests for words will then have a latency of up to 2 msec due to the circulation time of the memory. Waveform W45 shows the output strobe pulse.

Code Converter

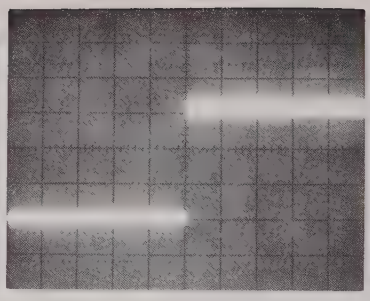
Gates A14 and A15 comprise a code converter to convert the Gray Code used in the ADC and memory to binary. The gates are exclusive "Or" gates which are connected in a ladder network. Gate A15 is used for the four most significant bits and gate A14 for the four least significant bits. Waveforms W37 - W44 show the data output with a full scale ramp input.

Time Switch Storage

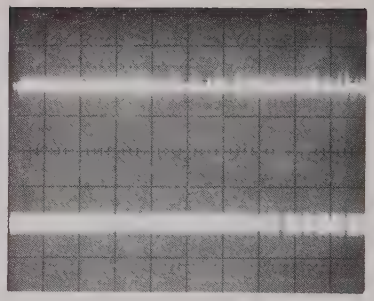
Memory A5 and its associated circuitry is used to store the time switch point in the Switched Time Base mode of operation. Input T2 is normally low but when the instrument switches from sweep time A to sweep time B, T2 goes positive. When T2 is low, all points of data will be stored as 0's. When T2 is high, all points will be stored as 1's. The time switch data is clocked out with the digital data and is used in two ways: as a reference to indicate when the time base switch occurred; and to enhance the Z output for X-Y display. (Waveform W36)



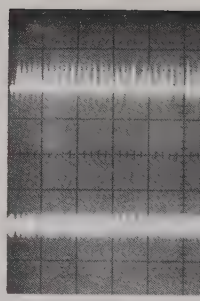
735 Clock 1/Clock 2.
oc: left lead of R29 & R30.
Scope: CH 1 5 V/div, CH 2 5 V/
iv. Horz: 1 µs/div. trig. on
lock 1. 802: trig. hold-off
ode. Single sweep.



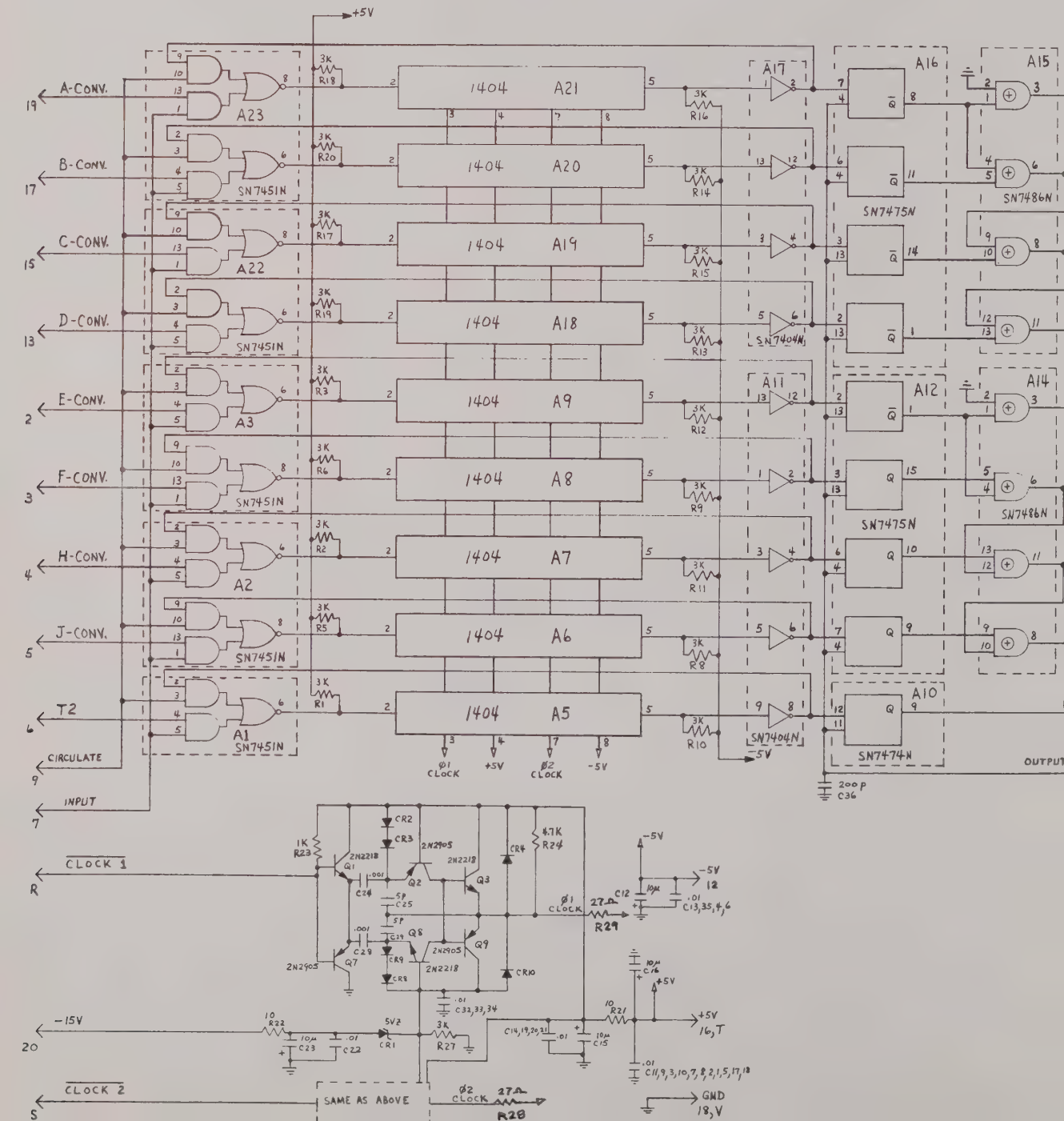
W36 Enhance. Loc: A10 pin 9.
Scope: 1 V/div. Horz: 0.2 ms/
div. ext. trig. on Z output.
802: switched time base mode.
Single Sweep delay approx. 2.70.

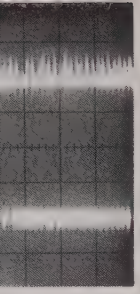


W37 $Y2^0$. Loc: A14 pin 8.
Scope: 1 V/div. Horz: 0.2 ms/
div. ext. trig. on Z output.
802: trig. hold-off mode.
Sweep time 500 µs single sweep
input 500 s ramp.

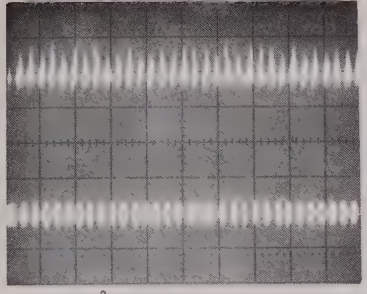


W38 $Y2^1$. Loc:
Scope: 1 V/div.
div. ext. trig.
802: trig. hold-
Sweep time 500 µ
input 500 µs ram

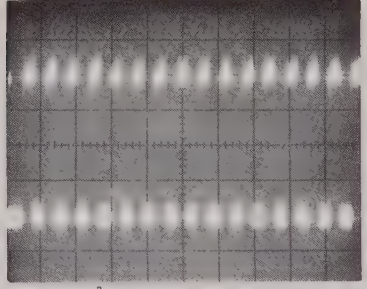




4 pin 11.
rz: 0.2 ms/
Z output.
f mode.
single sweep



W39 $Y2^2$. Loc: A14 pin 6. Scope: 1 V/div. Horz: 0.2 ms/ div. ext. trig. on Z output. 802: trig. hold-off mode. Sweep time 500 µs single sweep input 500 µs ramp.



W40 $Y2^3$. Loc: A14 pin 1. Scope: 1 V/div. Horz: 0.2 ms/ div. ext. trig. on Z output. 802: trig. hold-off mode. Sweep time 500 µs single sweep 500 µs ramp.

Y-2^7 → J

Y-2^6 → K

Y-2^5 → M

Y-2^4 → L

Y-2^3 → C

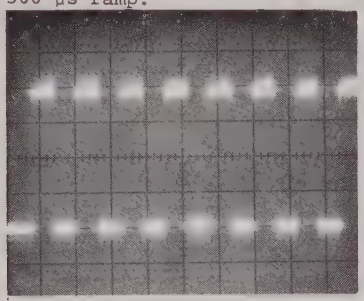
Y-2^2 → B

Y-2^1 → D

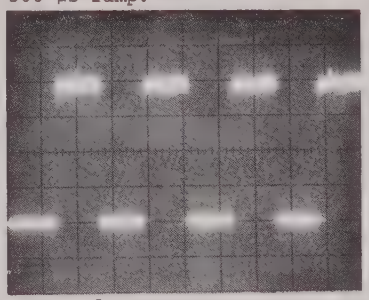
Y-2^0 → E

NHANCE → H

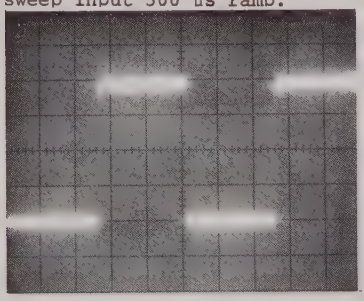
STROBE → P



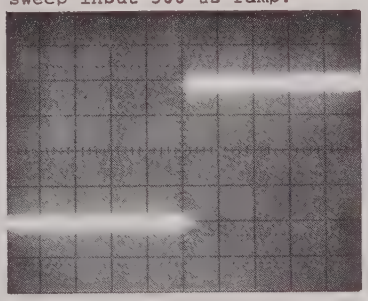
W41 $Y2^4$. Loc: A15 pin 11. Scope: 1 V/div. Horz: 0.2 ms/ div. ext. trig. on Z output. 802: trig. hold-off mode. Sweep time 500 µs X1, single sweep input 500 µs ramp.



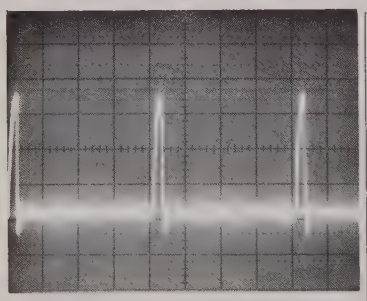
W42 $Y2^5$. Loc: A15 pin 8. Scope: 1 V/div. Horz: 0.2 ms, div. ext. trig. on Z output. 802: trig. hold-off mode. Sweep time 500 µs X1, single sweep input 500 µs ramp.



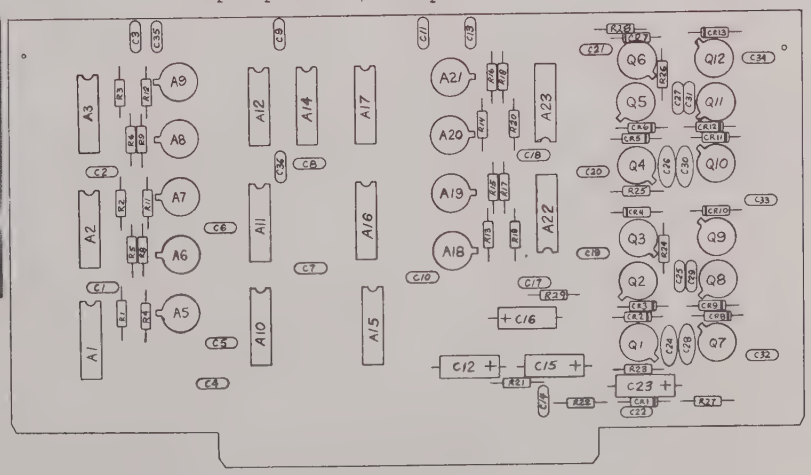
W43 $Y2^6$. Loc: A15 pin 6. Scope: 1 V/div. Horz: 0.2 ms/ div. ext. trig. on Z output. 802: trig. hold-off mode. Sweep time 500 µs X1, single sweep input 500 µs ramp.



W44 $Y2^7$. Loc: A15 pin 3. Scope: 1 V/div. Horz: 0.2 ms/ div. ext. trig. on Z output. 802: trig. hold-off mode. Sweep time 500 µs X1, single sweep input 500 µs ramp.



W45 Output Strobe. Loc: A10 pin 11. Scope: 1 V/ div. Horz: 0.5 µs/div. int. trig. 802: trig. hold-off, single sweep.



— MEMORY

Schematic & Assembly Drawing

LINEAR BOARD

The linear board performs a variety of functions in the Model 802. These functions include: the Y digital-to-analog conversion, X ramp generation, trigger discrimination, delay generation, and Z modulation and Enhance capabilities.

Y Digital-to-Analog Converter

The outputs from the code converter located on the memory board are connected to open collector inverters A2 and A3. The outputs of these inverters are then fed to a current mode switching type of digital-to-analog converter. There are three adjustments in this converter. Potentiometers R26 and R25 provide adjustment of the most significant bit and the second most significant bit. Potentiometer R27 provides a control for the three least significant bits. The output of the digital-to-analog converter is connected to the inverting input of a fixed gain operational amplifier. The wiper of the vertical position control located on the front panel is fed to the inverting input of this amplifier. The output of the amplifier is connected to the Y output. Waveform W47 shows a typical output. Transistors Q1 and Q2 provide a control output for the plot output. During times when the Model 802 is not in the Plot mode, the plot output is grounded by Q1. When the Plot mode is initiated, this ground is disabled and the plot output follows the Y output.

X Ramp Generation

The X ramp generator is an operational integrator comprised of transistors Q6, Q7 and Q8, and operational amplifier A9. AC advance pulses are amplified by Q6 and fed through a capacitor diode coupling network to the inverting input of A9. The output of A9 is fed back to the inverting input through integrating capacitor C25 to provide a ramp type signal out of the amplifier (Waveform W47). The horizontal position control located on the front panel is tied to the non-inverting input of A9. Potentiometer R88 controls the amplitude of the ramp generated by A9. The CRT input is used to turn off the ramp generator during the record cycle. The CRT signal is used to synchronize the ramp with the circulation of the memory in display. In display CRT is a 32 μsec wide pulse occurring every 2 msec. This pulse is amplified by transistor Q8 and fed to the gate of an FET switch Q7. This switch turns off the ramp output during times when the CRT pulse is low by shorting the feedback capacitor C25. The output level of the horizontal amplifier is 10 V p-p. Waveform W47 shows the relationship between the AC advance pulse and the horizontal ramp output. Waveform W48 shows the CRT pulse and the ramp reset in synchronization.

Trigger Circuit

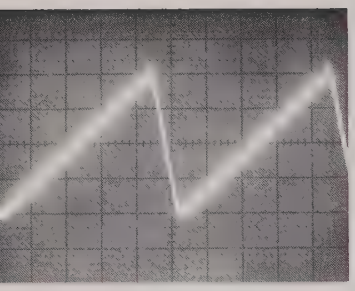
The trigger discriminator circuit is comprised of amplifiers A6 and A7, and gate A8. The trigger signal coming from the front panel is connected to the input of a unity gain amplifier A7. Diodes CR12 and CR21 provide a +15 V clamp to the input. The output of A7 is connected to the non-inverting input of operational amplifier A6. Amplifier A6 is a high gain amplifier of the same type used in the first rank analog-to-digital converter. The trigger level input from the trigger level potentiometer (located on the front panel) is applied to the inverting input of A6. When the input at A6 pin 5 exceeds the level of the input at A6 pin 6, the output (pin 8) will go positive. Waveform W49 shows the relationship between a trigger input signal and the output of the trigger discriminator inverted by A8. Gate A8 is an exclusive "Or" gate with pin 9 either at +5 or at ground, determined by the setting of the slope switch on the front panel. With gate A8 pin 9 at +5 V, the output of A6 is not inverted by A8. With the input of pin 9 of A8 at ground, the output of A6 will be inverted by A8.

Delay Generator

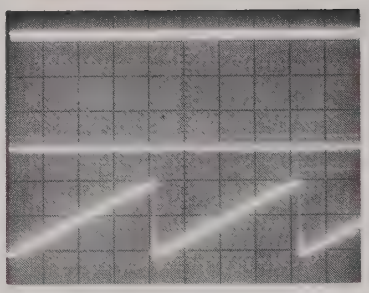
The delay circuit utilizes the time base to generate a voltage, which increases at a linear rate, for use in generation of the time delay. The time base is amplified by transistor Q3 and fed into a "pump" circuit composed of CR9, C12 and C7. Capacitor C7 is switched into the circuit by relay RY1, during times when the Model 802 is in interlace, to increase the delay time (Waveform W50). The output of amplifier A5 is fed to the discriminator amplifier A6 which compares the voltage set by the delay control on the front panel to the output voltage of amplifier A5. When the output of amplifier A5 applied to pin 12 of amplifier A6 exceeds the level set by the front panel controls, the output of A6 will go positive. The positive transition of A6 output is shaped by A8 and A4 and becomes the End of Delay pulse ($\overline{\text{EOD}}$), which resets flip-flop A4 which was set by the start of delay pulse, thus ending the delay cycle. When the end of delay pulse occurs, the pump capacitor is discharged by FET switch Q5 through transistor Q4. Waveform W50 shows the time base input and A5 output. Waveform W51 shows the relationship between A5 output and the delay output. Waveform W52 shows the start of delay and end of delay pulses.

Enhance

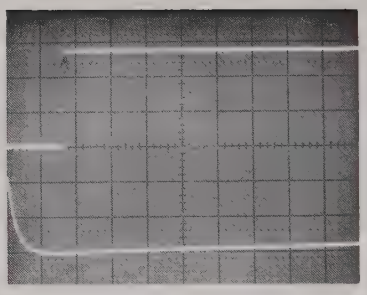
The enhance circuit uses the CRT pulse to generate the Z and $\overline{Z}$ outputs used for CRT blanking and oscilloscope triggering. The "bright output" from the memory board, which is the time switch point in the Switched Time Base mode, is mixed with these two signals to produce the Enhance output for Z modulation in Switched Time Base mode. Waveform W53 shows the relationship between the CRT signal and the bright output signal, with the unit in the Switched Time Base mode of operation. Waveform W54 shows the relationship of the Z out and $\overline{Z}$ outputs in the Switched Time Base mode. During blanking both the Z output and the $\overline{Z}$ output are at ground.



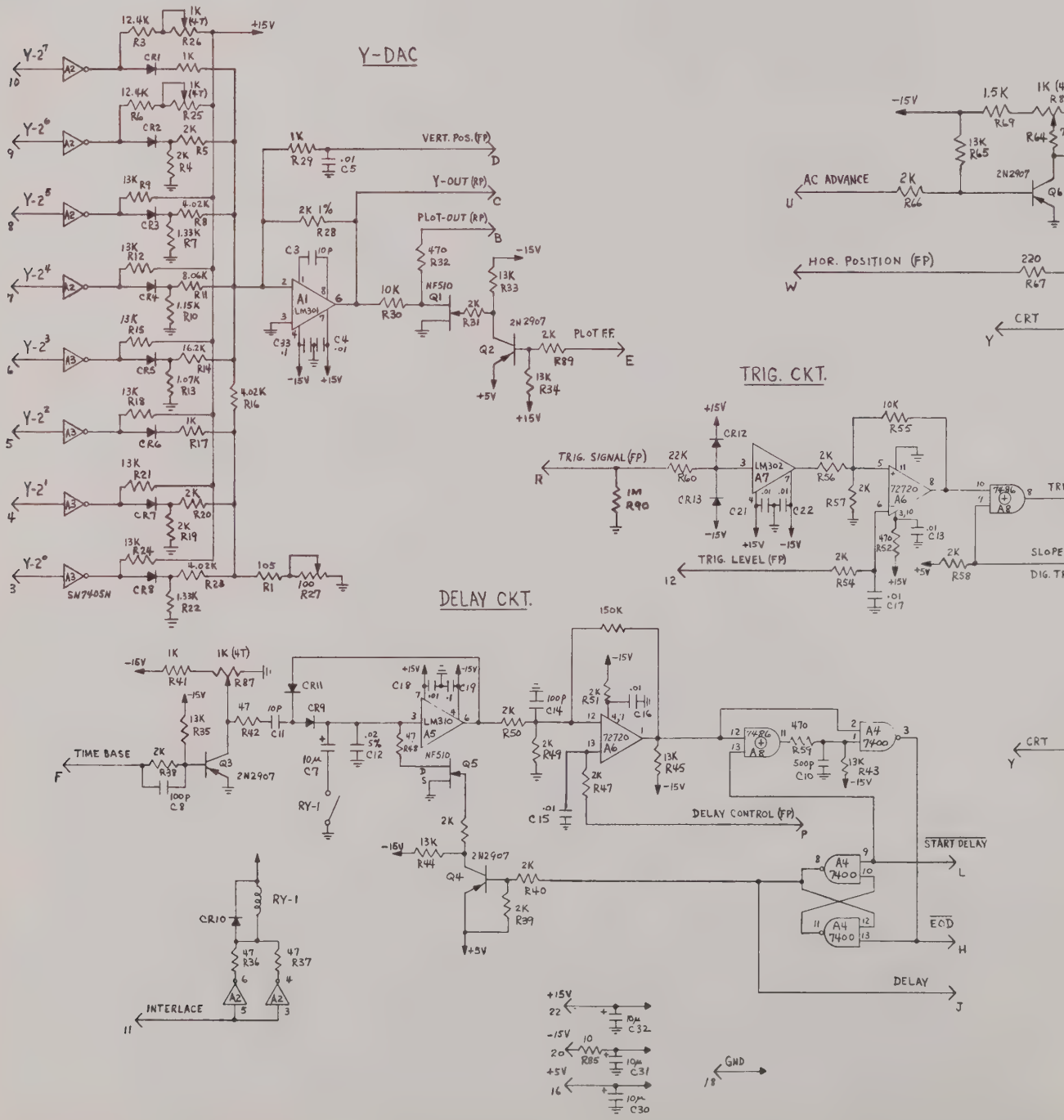
W46 Y Output. Loc: A1 pin 6. Scope: 1 V/div. Horz: 0.2 ms/ div. trig. on Z output. 802: sweep time 500 µs X2. Trig. holdoff mode, single sweep, input 500 µs ramp input.

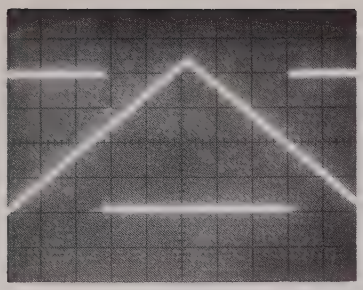


W47 AC Advance/Horiz. Output Loc: Board pin U/A9 pin 6. Scope: CH 1 1 V/div, CH 2 5 V/ div. Horz: 0.5 ms/div, trig. on CH 2. 802: trig. holdoff mode. Single sweep (display).

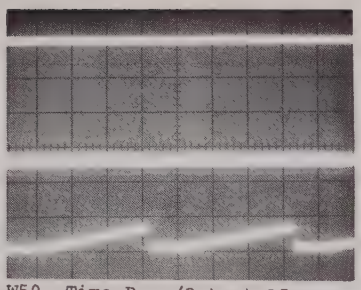


W48 CRT/Horiz. Output Reset Loc: Board pin Y/A9 pin 6. Scope: CH 1 2 V/div, CH 2 5 V/ div. Horz: 20 µs/div, trig. on CH 1. 802: trig. holdoff mode. Single sweep (display).

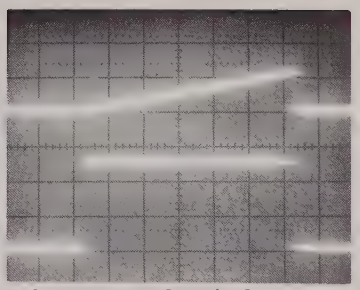




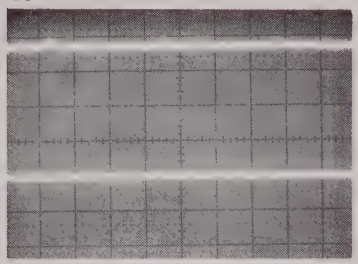
W49 Trig. Signal/Trigger
Loc: Board pin R/A8 pin 8.
Scope: CH 1 1 V/div, CH 2 1 V/div. Horz: 50 µs/div, trig. on CH 1. 802: triangle input to trigger input 5 V p-p.



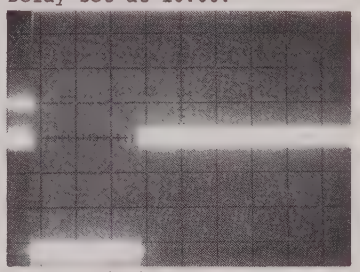
W50 Time Base/Output A5
Loc: Board pin F/A5 pin 6.
Scope: CH 1 1 V/div, CH 2 2V/div. Horz: 1 ms/div, trig. on CH 2. 802: delayed sweep mode. Normal trigger. Delay set approx. 3.00.



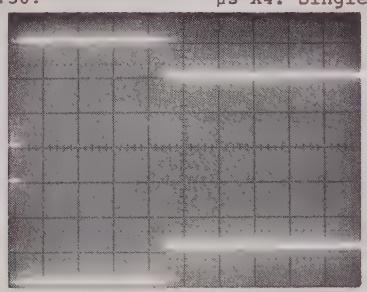
W51 Output of A5/Delay.
Loc: A5 pin 6, A4 pin 8. Scope: CH 1 2 V/div, CH 2 5 V/div. Horz: 1 ms/div, trig. on delay. 802: trig. holdoff. Normal trig., sweep time 500 µs X1. Delay set at 10.00.



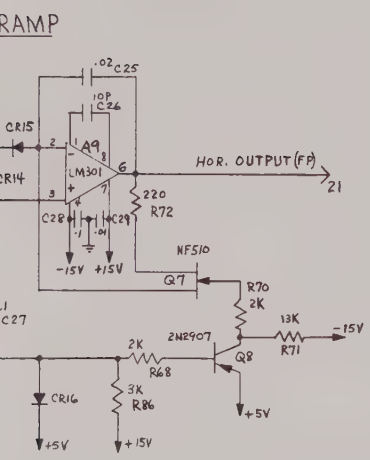
W52 $\overline{\text{EOD}}$/Start Delay
Loc: A4 pin 13/A4 pin 9.
Scope: CH 1 2 V/div. Horz: 10 µs/div, trig. on CH 2. 802: Trig. holdoff, sweep time 500 µs X1. Norm. trig. Delay set at approx. 0.30.

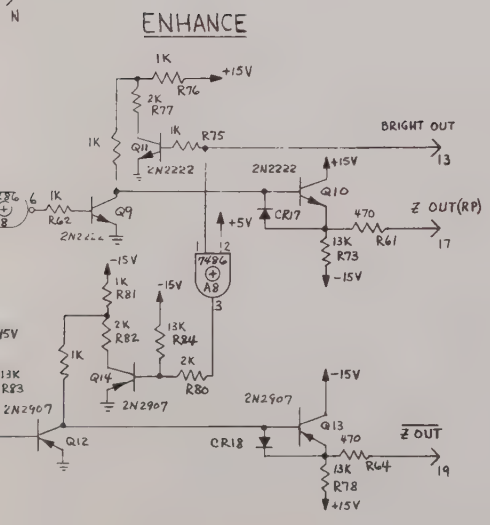


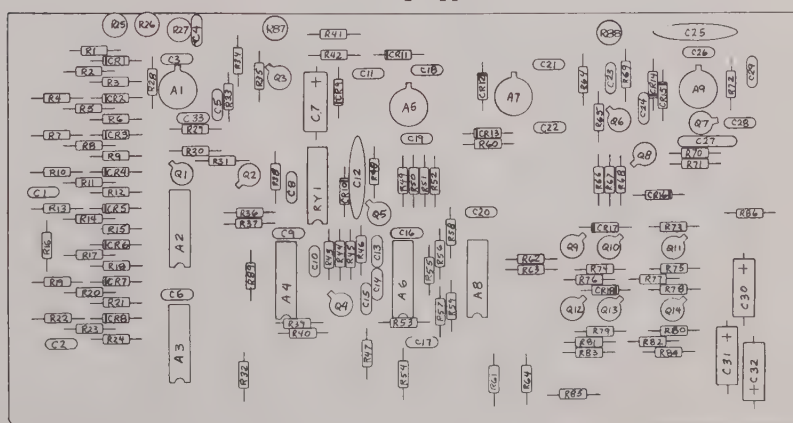
W53 CRT/Bright Out.
Loc: A8 pin 4/A8 pin 1.
Scope: CH 1 2 V/div, CH 2 2 V/div. Horz: 50 µs/div. trig. on CH 1. 802: switched time base. Sweep time A 500 µs X1, B 500 µs X4. Single. Delay app. 1.00.



W54 Z Output/$\overline{\text{Z}}$ Output. Loc: Board pin 17/Board pin 19.
Scope: CH 1 5 V/div, CH 2 5 V/div. Horz: 0.2 ms/div. trig. on CH 1. 802: sw. time base. Single. Swp. time A 500 µs X1, B 500 µs X4. Delay app. 2.50.







LINEAR

Schematic & Assembly Drawing

TIME BASE & ADDRESS BOARD

The time base and address board provides generation of all the necessary clock and time base frequencies for control of the instrument during Record and Display. The memory tracking counters AC and M are located on this board.

AC & M Counter

Both the AC counter (A17, A30 and A20) and the M Counter (A28, A29 and A9) are 10 bit binary counters. Between these two counters are a row of comparators which are exclusive "Or" gates whose outputs are diode-coupled to the input of an additional exclusive "Or" gate which produces the AC = M signal. The AC counter is advanced at the same rate the memory is clocked. The M counter, during Record, is advanced at the same rate as the AC counter except during interlace. In Record-Interlace, the AC counter is advanced at a faster rate and the M counter is advanced each time the AC counter overflows. This combination causes the M counter to advance consistent with the sweep time setting. At each coincidence of AC and M, new data is inserted into the memory. Waveform W55 shows the relationship between AC and M during Record in non-interlace. Waveform W56 shows the relationship between AC and M in interlace. Waveform W57 shows the relationship between the AC advance and the "512" output. Waveform W58 shows the relationship between the Z output and the 512 output. Waveform W59 shows the relationship between the AC = M pulse and the AC advance pulse.

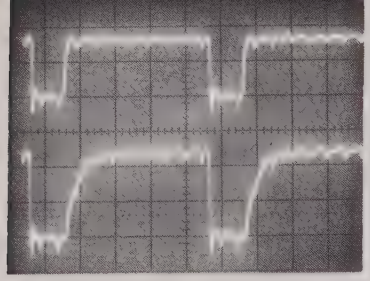
Time Base Generation

Time base generation is accomplished by a 10 MHz crystal controlled oscillator comprised of gates A10 and the crystal Y1. The output of this oscillator is used for the clock input on the control boards and is fed to a series of seven decade dividers. The outputs of the dividers are gated by A10, A13 and A14 to a ÷5 counter. The output of the ÷5 counter is fed to a ÷2 counter, A26. A26 drives another ÷2 counter, A27. The outputs of these two counters are gated by A25 and A14 to the time base output. Control for the time base is derived from the resistor network which can either be driven from the front panel with the sweep time controls or be driven from an external devide through the rear panel connector J9. The X4 position is determined by gate A22. If the Model 802 is not in X1 or X2, the output of A22 pin 3 is true and, therefore, the time base is divided by 4. Upon initiation of a record or output cycle, the entire time base is reset by the Time Base Reset line. The time base provides the 1 msec time base used for the control logic, the plot time base (which is the output of A5 shaped by gate A15) and the display time base. The specific

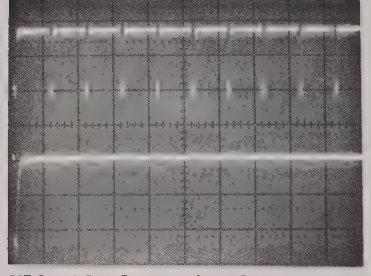
time base output repetition rates and frequencies for all sweep time positions are given in the Calibration section of this manual. The Waveform W60 shows the relationship between the clock output and the time base output at the 500 μsec sweep speed. Waveform W61 shows the relationship between the clock and the display time base.

Plot Output Rate

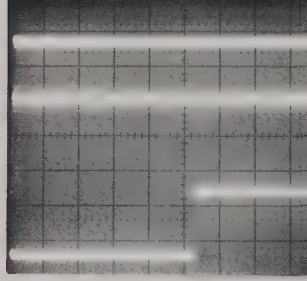
A speed change option is provided at the output of A5. This option is normally wired in the 0.1 sec position but may be changed to the 0.2 or 0.5 sec position by adding a wire jumper. The output rate can also be increased by a factor of 10 by removing decade divider A4 and jumpering terminal a on the circuit board to pin 12 of A14.



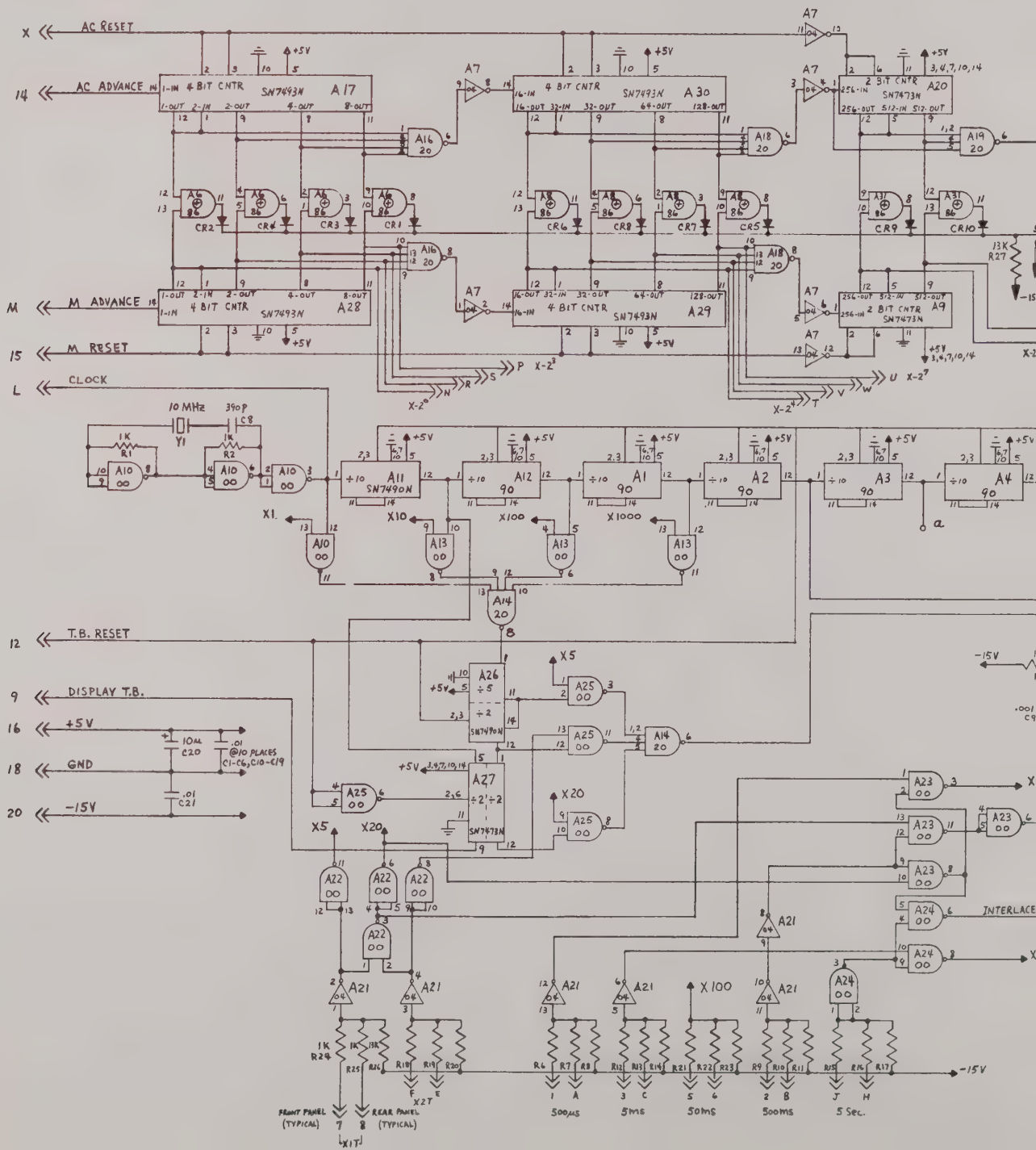
W55 AC Advance/M Advance. (non-interlace) Loc: A17 pin 14/A28 pin 14. Scope: CH 1 2 V/ div, CH 2 2 V/div. Horz: 0.2 µs /div, trig. on CH 1. 802: pre-trigger record. Sweep time 500 µs X2.

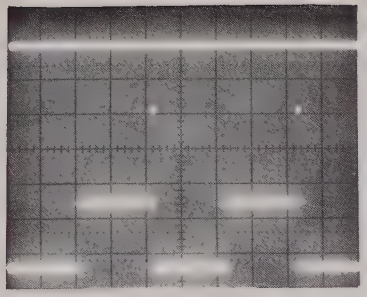


W56 AC Advance/M Advance (interlace). Loc: A17 pin 14/ A28 pin 14. Scope: CH 1 2 V/ div, CH 2 2 V/div. Horz: 2 µs/ div, trig. on CH 2. 802: pre-trigger record. Sweep time 500 ms X4.

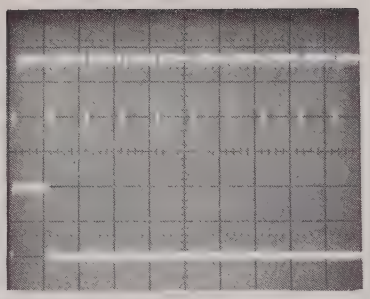


W57 AC Advance/Count 512 put. Loc: A17 pin 14/A20 Scope: CH 1 2 V/div, CH 2 div. Horz: 50 µs/div, trig CH 2. 802: pretrigger rec Sweep time 500 µs X1.

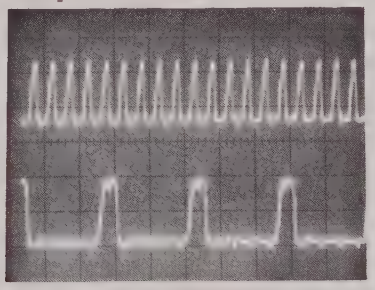




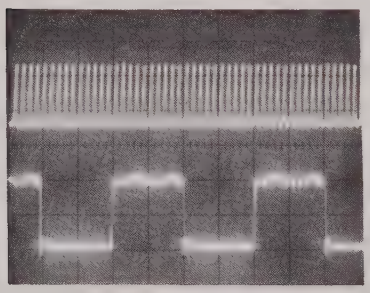
W58 Z Output/512 Count.
Loc: A19 pin 6/A20 pin 9.
Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 0.5 ms/div, trig. on CH 1. 802: trig. holdoff. Single sweep (display).



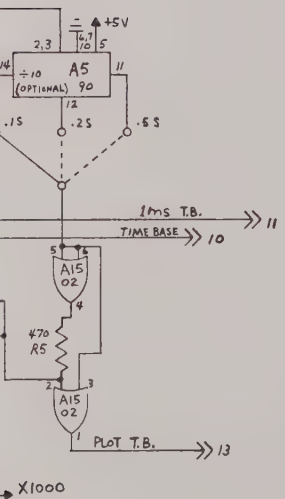
W59 AC = M/AC Adv (interlace)
Loc: A31 pin 6/A17 pin 14.
Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 2 µs/div, trig. on CH 1. 802: pretrig. record. Sweep time 500 ms X4.

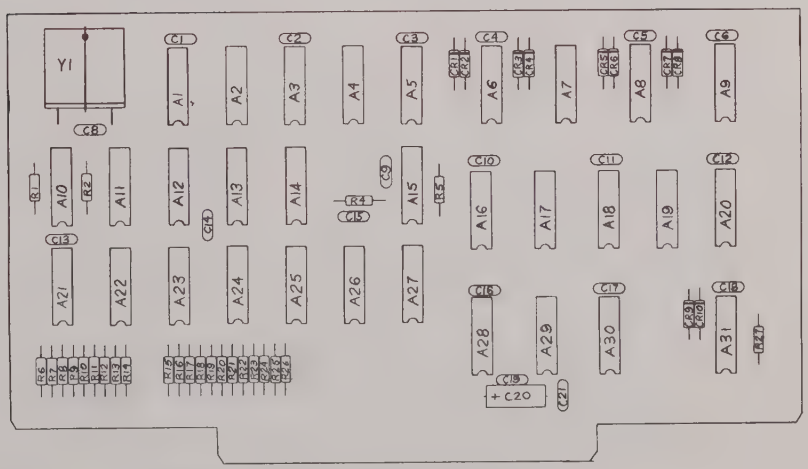


W60 Clock/Time Base.
Loc: A10 pin 3/Board pin 10.
Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 0.2 µs/div, trig. on CH 2. 802: sweep time 500 µs X1.



W61 Clock/Display Time Base.
Loc: A10 pin 3, Board pin 9.
Scope: CH 1 2 V/div, CH 2 2 V/ div. Horz: 0.5 µs/div, trig. on CH 2.





TIME BASE & ADDRESS

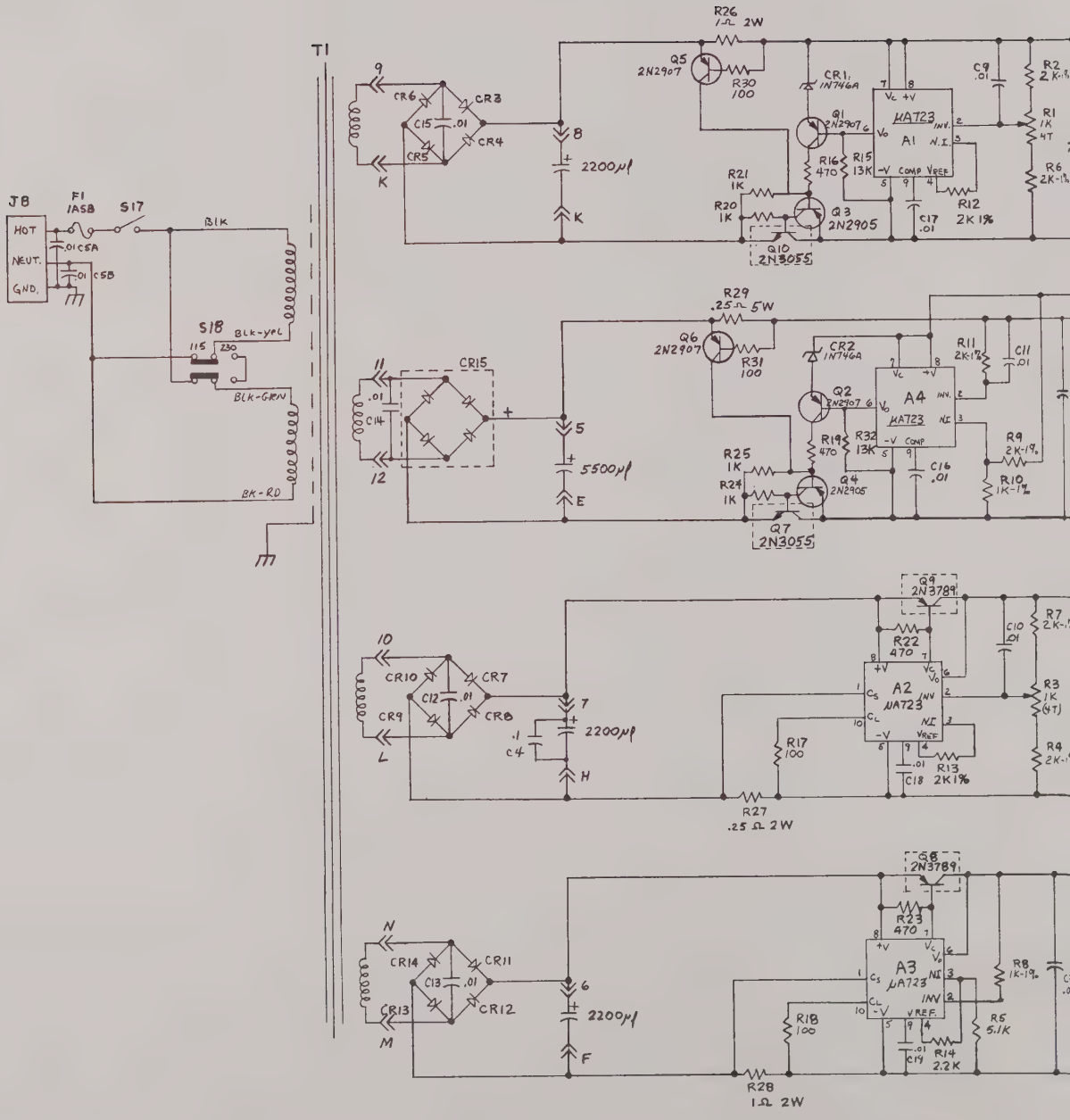
Schematic & Assembly Drawing

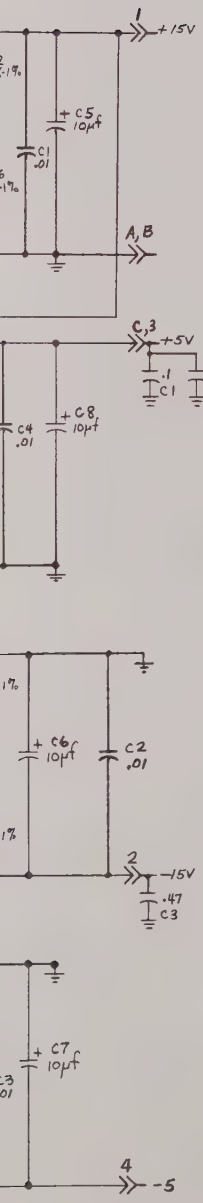
POWER SUPPLY

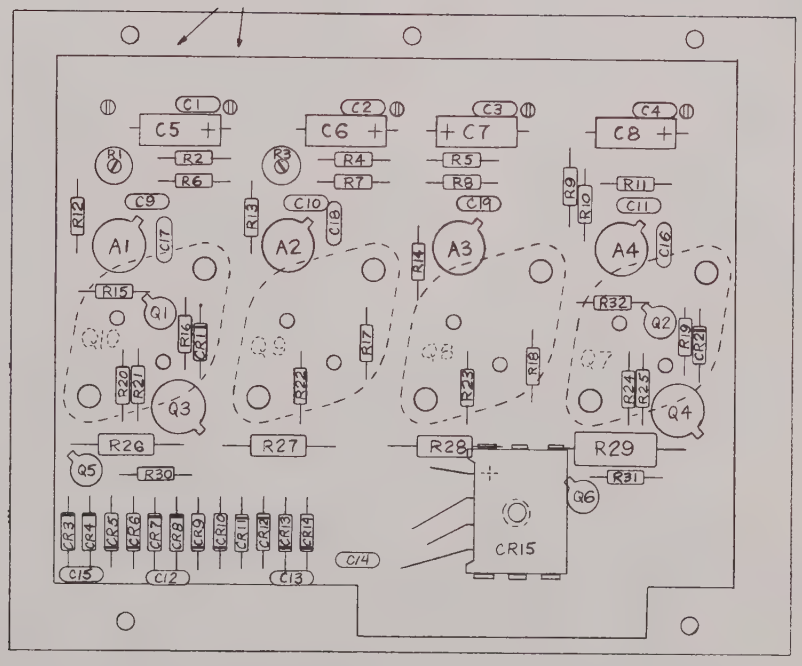
There are four power supplies used in the Model 802. They are the +15 V, -15 V, -5 V and +5 V. These power supplies are all series regulated utilizing grounded-collector series-pass transistors and integrated circuit regulators. All four power supplies are equipped with a current limiting feature. If the output of the power supply is shorted or the amount of current flow exceeds that normally used in the Model 802, the power supply output voltage drops to zero. During normal operation, the following currents are being drawn out of the power supplies:

+15 V	0.6 amp
-15 V	0.3 amp
-5 V	0.2 amp
+5 V	1.8 amp

Voltage adjustments are provided on the +15 V and -15 V power supplies. The +5 V power supply is referenced to the +15 V power supply and no adjustment of the +5 V is necessary since the two power supplies will track each other. The -5 V power supply is a fixed voltage power supply in that fixed resistors are used to set the output level.

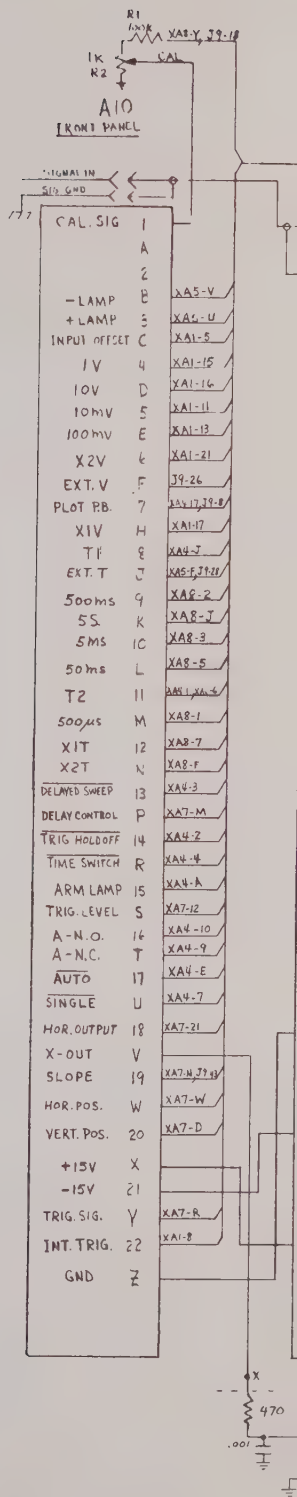

J8
HOT
NEUT.
GND.
F1
1ASB
S17
.01 C5A
.01 C5B
BLK
S18
115
230
BLK-YEL
BLK-GRN
BK-RD
T1
9
K
CR6
CR3
CR5
CR4
C15 .01
8
2200µf
K
R26 1Ω 2W
Q5 2N2907
R30 100
CR1 1N746A
Q1 2N2907
R16 470
R15 13K
R21 1K
R20 1K
Q3 2N2905
Q10 2N3055
MA723
A1
N.I.
-V COMP VREF
C17 .01
R12 2K 1%
C9 .01
R2 2K-1%
R1 1K
R6 2K-1%
11
12
CR15
C14 .01
5
5500µf
E
R29 .25Ω 5W
Q6 2N2907
R31 100
CR2 1N746A
Q2 2N2907
R19 470
R32 13K
R25 1K
R24 1K
Q4 2N2905
Q7 2N3055
A4
MA723
COMP
C16 .01
R11 2K-1%
C11 .01
R9 2K-1%
R10 1K-1%
10
L
CR10
CR7
CR9
CR8
C12 .01
7
.1 C4
2200µf
H
Q9 2N3789
R22 470
A2
µA723
R17 100
R27 .25Ω 2W
C10 .01
R7 2K-1%
R3 1K (4T)
R4 2K-1%
R13 2K 1%
C18 .01
N
M
CR14
CR11
CR13
CR12
C13 .01
6
2200µf
F
Q8 2N3789
R23 470
A3
µA723
R18 100
R28 1Ω 2W
R8 1K-1%
R5 5.1K
R14 2.2K
C19 .01

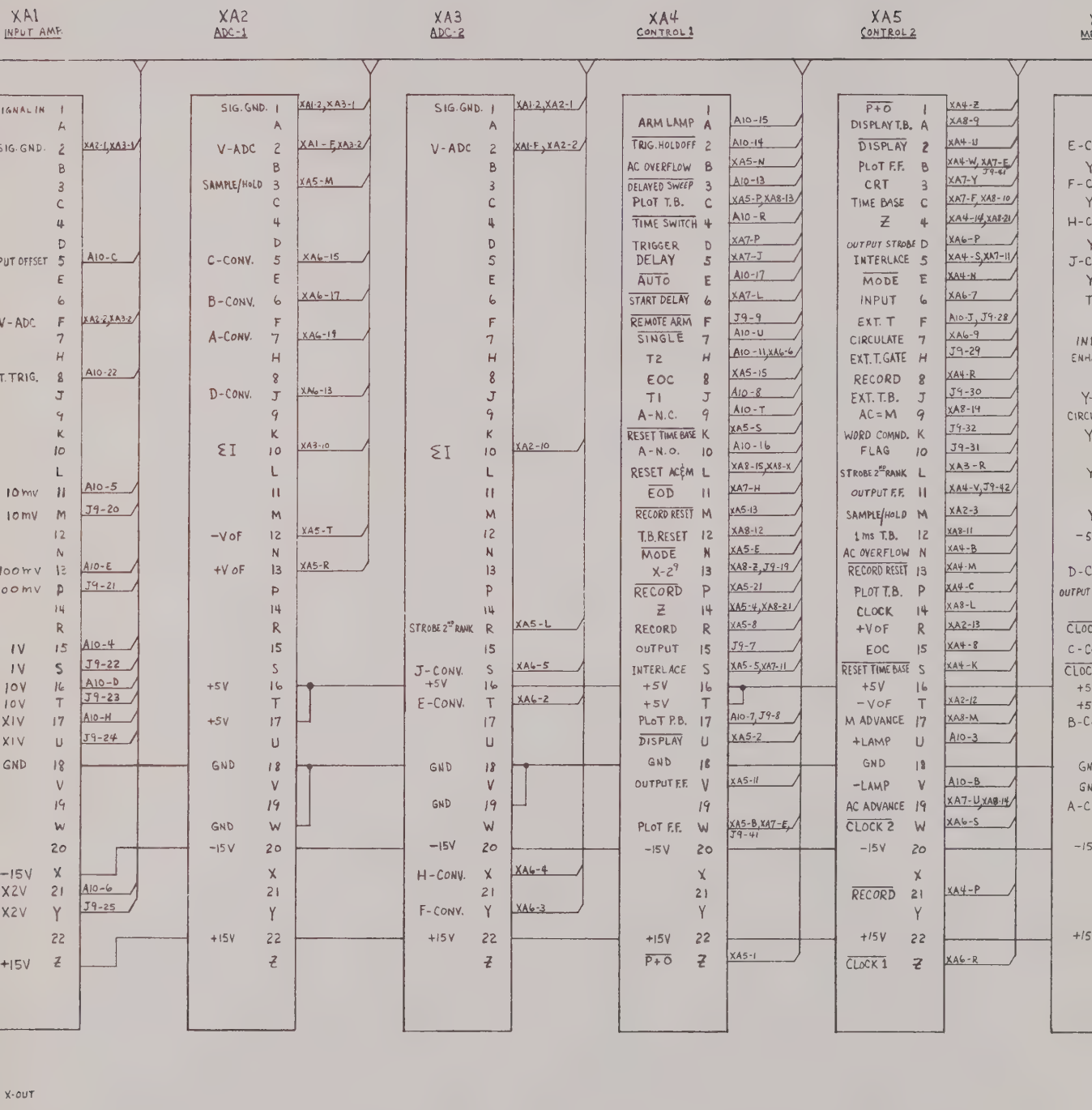




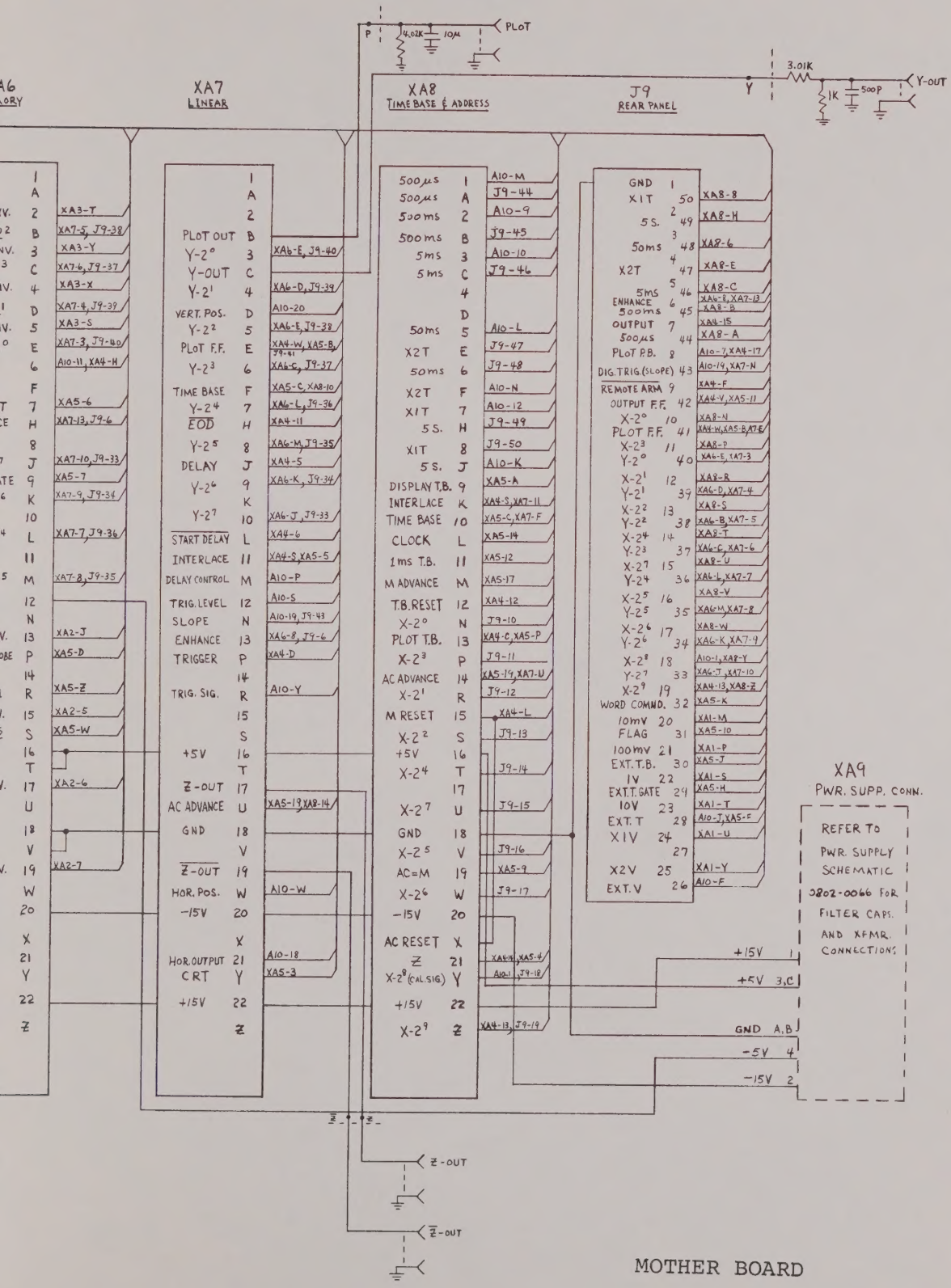
POWER SUPPLY

Schematic & Assembly Drawing


R1
1K
XA8-Y, J9-18
1K
R2
CAL
A10
FRONT PANEL
SIGNAL IN
SIG GND
CAL. SIG 1
A
2
-LAMP B XA5-V
+LAMP 3 XA5-U
INPUT OFFSET C XA1-5
1V 4 XA1-15
10V D XA1-16
10mV 5 XA1-11
100mV E XA1-13
X2V 6 XA1-21
EXT. V F J9-26
PLOT P.B. 7 XA1-17, J9-8
X1V H XA1-17
TF 8 XA4-J
EXT. T J XA5-F, J9-28
500ms 9 XA8-2
5S. K XA8-J
5MS 10 XA8-3
50ms L XA8-5
T2 11 XA1, XA4-6
500μs M XA8-1
X1T 12 XA8-7
X2T N XA8-F
DELAYED SWEEP 13 XA4-3
DELAY CONTROL P XA7-M
TRIG HOLDOFF 14 XA4-2
TIME SWITCH R XA4-4
ARM LAMP 15 XA4-A
TRIG. LEVEL S XA7-12
A-N.O. 16 XA4-10
A-N.C. T XA4-9
AUTO 17 XA4-E
SINGLE U XA4-7
HOR. OUTPUT 18 XA7-21
X-OUT V
SLOPE 19 XA7-N, J9-23
HOR. POS. W XA7-W
VERT. POS. 20 XA7-D
+15V X
-15V 21
TRIG. SIG. Y XA7-R
INT. TRIG. 22 XA1-8
GND Z
X
470
.001


XA1
INPUT AMP.
XA2
ADC-1
XA3
ADC-2
XA4
CONTROL 1
XA5
CONTROL 2
SIG. GND.
V-ADC
SAMPLE/HOLD
C-CONV.
B-CONV.
A-CONV.
D-CONV.
ΣI
-VOF
+VOF
+5V
GND
-15V
J-CONV.
E-CONV.
H-CONV.
F-CONV.
+15V
ARM LAMP
TRIG. HOLDOFF
AC OVERFLOW
DELAYED SWEEP
PLOT T.B.
TIME SWITCH
TRIGGER DELAY
AUTO
START DELAY
REMOTE ARM
SINGLE
T2
EOC
T1
A-N.C.
RESET TIME BASE
A-N.O.
RESET ACCUM
EOD
RECORD RESET
T.B. RESET
MODE
X-2^9
RECORD
Z
RECORD
OUTPUT
INTERLACE
PLOT F.F.
DISPLAY T.B.
DISPLAY
PLOT F.F.
CRT
TIME BASE
Z
OUTPUT STROBE
INTERLACE
MODE
INPUT
EXT. T
CIRCULATE
EXT. T. GATE
RECORD
EXT. T.B.
AC=M
WORD COMND.
FLAG
OUTPUT F.F.
SAMPLE/HOLD
1 ms T.B.
AC OVERFLOW
RECORD RESET
PLOT T.B.
CLOCK
+VOF
EOC
RESET TIME BASE
-VOF
M ADVANCE
+LAMP
-LAMP
AC ADVANCE
CLOCK 2
CLOCK 1

X-OUT



MOTHER BOARD

Schematic Diagram

7.11

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